Trends in Consumer CMOS Image Sensor Manufacturing

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Overview

Mature semiconductor sectors, such as microprocessors and memory, once enjoyed a high number of entrepreneurial players during the growth phase of their markets. Market pressures ultimately forced consolidation, leaving only a few innovative companies intact to dominate a sector. History and economics suggest commoditization of CMOS image sensors (CIS) is inevitable. This phenomenon has not yet occurred within the CIS sector due to the diversity in end use applications. Instead of the over 50 CIS players battling for similar sockets, each have traditionally leveraged their expertise in one or a few of nine distinct subsectors. These subsectors comprise: camera phone/mobile device, digital single lens reflex (DSLR), digital still camera, consumer HD video, cinema HD video, automotive/security, 3D imaging, scientific/industrial, and aerospace/military.

The current economic downturn presents new challenges to all CIS providers and consumer demand for crossover products threatens to blur the line between subsectors. In the face of such challenges, the small pixel CIS leaders continue to incorporate innovative process and design features in their sensors. These innovations offer true product differentiation, and enable market share retention and growth. Chipworks is a technology consulting company that has expertise in monitoring successful CIS technologies employed in the small pixel/camera phone, DSLR, and consumer HD video sectors. This paper will highlight selected trends of some leading innovators in the areas of pixel layout, back end of line (BEOL) fabrication process, and packaging.

The 1.75 µm Pixel Generation Trends

The 1.75 µm pixel generation has been implemented in 180 nm through 90 nm process technologies (Figure 1). The choice of technology generation (node) has implications for both the pixel array and SoC functionality. Logic scaling can either allow an increased SoC feature set or number of die per wafer. Deep submicron processes enable narrow metal wiring in the pixel array.

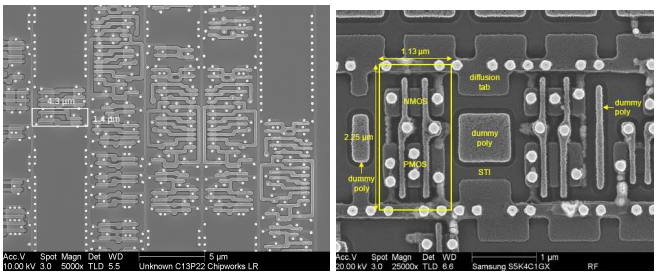

Figure 1: 1.75 µm Pixel SoC Imagers Implemented in 180 nm (Sharp) and 90 nm (Samsung) Process Nodes (Corresponding Standard Logic Cell Size of 6.0 µm^2 and 2.5 µm^2)

First generation 1.75 µm pixels typically used conventional (i.e., only electrically necessary) metal routing. Subsequent redesigns, and sensors from late entrants, focused on

improvements in optical symmetry by adding dummy metal in the optical path. Much effort was expended in symmetrical pixel design, resulting in up to three and four versions of 1.75 µm pixels from some of the leaders (Figures 2 and 3).

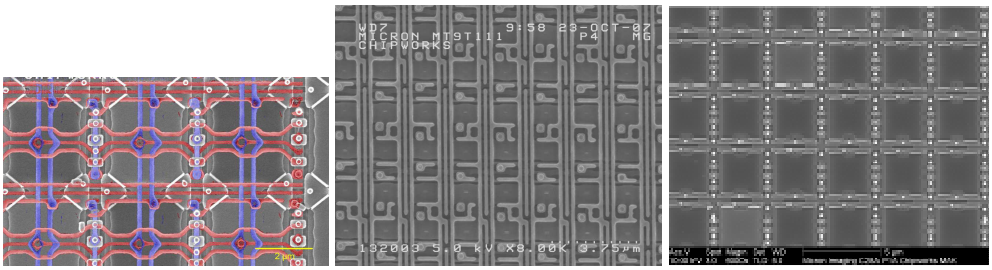

Figure 2: Three Iterations of the Micron 1.75 µm Pixels (Poly through Metal 2 Composite, at Metal 1, and at Poly)

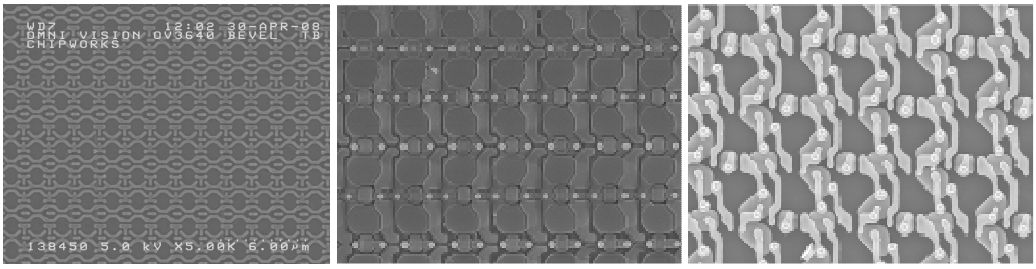

Figure 3: Two OmniVision 1.75 µm Pixels (at Metal 1 and Poly) and Toshiba 1.75 µm pixel (at Metal 1/Poly)

Pixel BEOL Trends

New for the 1.75 µm pixel generation, mask and process steps were added to reduce the dielectric stack thickness over the pixel array. Shared pixel designs and narrow metal lines also facilitated a two metal only pixel interconnect scheme (Figure 4).

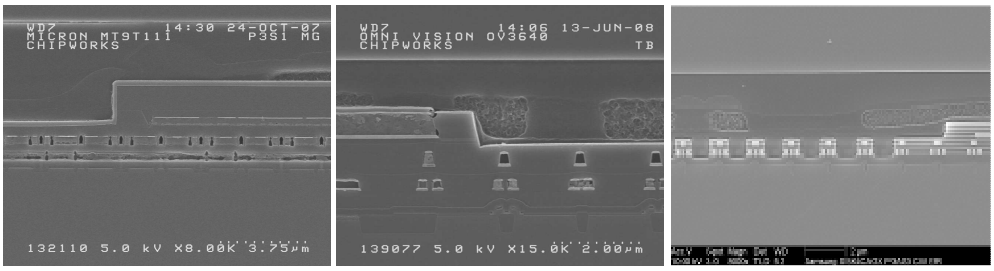

Figure 4: Reduced Interconnect, Thinned Optical Stack (Micron, OmniVision, and Samsung)

For some manufacturers, the transition from 2.2 µm to 1.75 µm pixels corresponded to a switch from Al to Cu BEOL processing. Three different techniques were used to remove the silicon nitride films, common to Cu processing, from the optical stack: optical waveguides (light pipes), mask-etch-fill of pixel cavities, and mask-etch of the metal capping dielectrics (Figure 5).

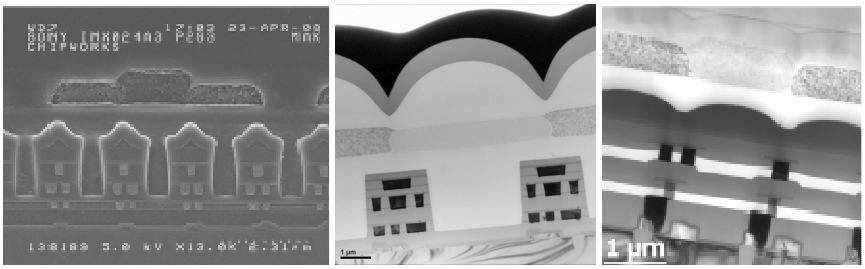

Figure 5: Light Pipes (Sony), Mask-Etch Fill Cavity (Samsung), and Mask-Etch Nitride Sealant (Canon)

Future Trends – 1.4 µm Pixel Generation, Backside Illuminated CIS

State of the art CIS's used in mobile devices are transitioning from the 1.75 µm to 1.4 µm generation pixels. At the paper submission deadline, the single 1.4 µm pixel CIS analyzed used second generation light pipes and an efficient clustered transfer transistor layout. The pixel interconnect was highly optimized for optical symmetry.

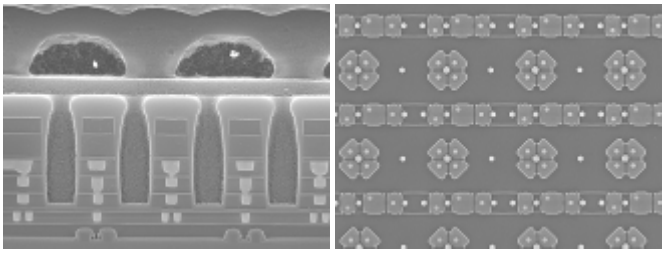

Figure 6: Sony 1.4 µm pixels (Light Pipes, Clustered Transfer Gates, and Dedicated V_{SS} Contact)

A paradigm shift is underway, as backside Illumination (BSI) technology hits the consumer electronics supply chain. The first BSI device analyzed was fabricated using several exotic fabrication processes, including substantial processing on both sides of a thin silicon substrate, backside wire bonding, adhesive-based wafer bonding, an unconventional pixel anti-reflective layer, and three types of isolation, amongst other features (Figure 7). This part, designed for use in consumer video applications, did not have the form factor restraints of a camera phone. Ultra slim mobile devices using BSI technology are expected to employ through silicon vias (TSVs).

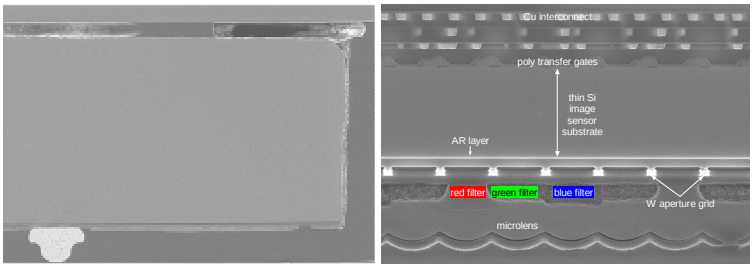

Figure 7: Sony BSI CIS Overview, Detail of BSI Sensor Substrate

Advanced Packaging Trends

Several advanced packaging techniques have come into production, to reduce both the module costs and the form factor. Wafer level chip scale packaging (WL-CSP) and TSVs have enabled significant reductions in the module form factor for mobile applications (Figures 8 and 9).

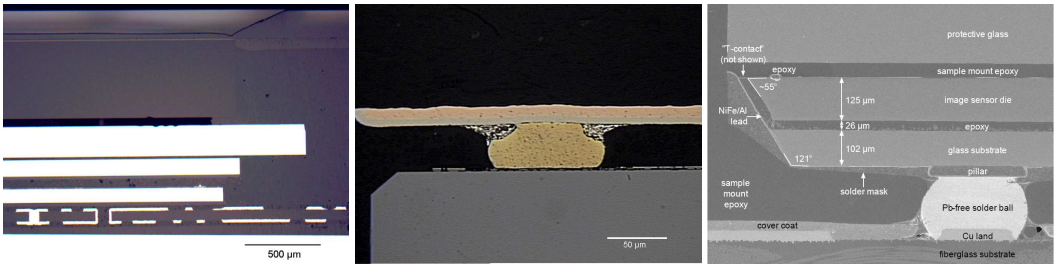

Figure 8: Co-Packaging (Sharp), Lead over Chip (Panasonic), WL-CSP (OmniVision)

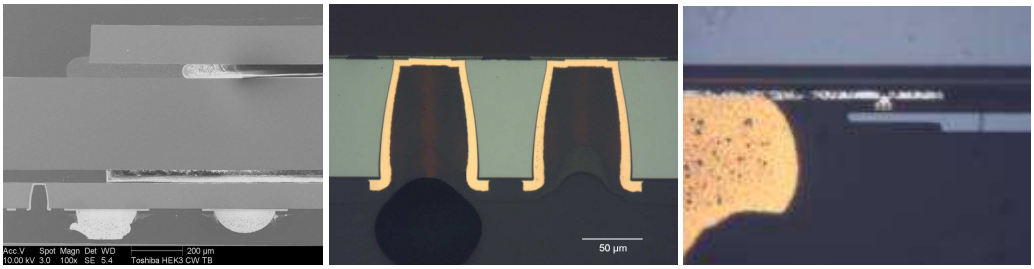

Figure 9: Through Silicon Vias (Toshiba), Backside Wire Bonding (Sony BSI)

Observations

- Advanced node fabrication (sub 0.13 µm) is becoming a requirement for small pixel front side illuminated (FSI) CIS
- Sophisticated BEOL processing and clever pixel wiring have allowed FSI sensors to meet performance requirements
- Both FSI and BSI sensors are in production or on corporate road maps for the 1.4 µm pixel generation
- The small pixel innovators appear to be a year or more ahead of the tier 2 providers, in terms of process development and pixel design
- Traditionally cost prohibitive advanced packaging techniques have made it into production

Author Biography

Ray Fontaine has been a process analyst at Chipworks since 2001, specializing in image sensors. He has authored and technically reviewed numerous image sensor process review (IPR) reports. Chipworks has produced over 100 detailed technical reports covering the process and circuit designs of image sensors from 17 companies. Contact the author to receive a copy of this paper and conference presentation (rfontaine@chipworks.com).