Pixel continues to shrink….
Pixel Development for Novel CMOS Image Sensors.

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Abstract

Modern trends in camera module designs for both mobile and DSC applications are driving ever smaller pixels. At the same time, higher demands on the quality of the output image (DSC-like quality for mobile applications) requires maintaining pixel capacity, quantum efficiency (QE), and sensitivity, which becomes extremely difficult as the pixel size shrinks. This paper discusses pixel designs and process enhancements that enable a new generation of Image sensors with 1.75um, 1.4um, and smaller pixels with superior performance. The paper presents simulation data and experimental optical-electrical characteristics of our latest generation of 1.4um and 1.75um pixels, as well as improvements in pixel performance made through new pixel architectures and process enhancements. The paper presents performance comparisons of image sensors with different pixel sizes and array formats for the popular mobile ¼ inch optical format including Aptina's newest 5Mpix sensor with 1.4um pixel size.

1. Pixel Optical Path and Si-Photodiode Enhancement

Optimization of the pixel optical path and Silicon photodiode structure is done via the "perfect pixel concept" that can be described shortly as follows:

- ✓ All light coming into the pixel needs to pass through the corresponding color filter (CF).
- ✓ A color filter should be optimized for the color reproduction as well as SNR, which means tuning of transmitting and blocking performances of the CF – optimization of CF material, thickness, and patterning process.
- ✓ All light that is passing through the CF should be delivered to the surface of PD without any loss.
- ✓ Finally, all light that came onto the PD must stay within the Si PD absorption box and be absorbed completely in this absorption box.

The advanced pixel optical path incorporates Aptina's 90nm Cu or Al metal back-end process, optimized color filters, dielectric light guide, and burried antireflective coating on the $Si\text{-}SiO_2$ interface.

Aptina's light guide is composed of material with an index of refraction higher than the surrounding oxide. The geometry of light guide, including length, shape, and size are carefully designed to allow maximal light coupling into the photodiode. Optimization of the light guide design and manufacturing process takes into account physical and thermal properties of light guide material as well as process features. Generally speaking, it's desired to bring output of the light guide as close to the Si surface as possible to avoid light scattering. However, this may increase the chance of etch damage to the photodiode surface thus introducing hot pixels. This concern has been resolved by using an etch stop layer ensuring the light guide terminates at the proper distance above silicon.

The size and shape of light guide play an important role in ability to work with high angles of light. It is found that the larger the top opening, the more angled light can be collected. Aptina's light guide is optimized for the best tradeoff between symmetry, green channel imbalance, and ability to couple light with different angles of incidence. The pixel related fix pattern noise (FPN) is another important aspect of light guide design. To minimize FPN, one has to ensure the light guide etch, fill, and chemical-mechanical polish (CMP) process are uniform across the pixel array. More important, there should be no cracking or delaminating of light guide material from the surrounding surfaces which can lead to non-uniform pixel response. The process compatibility with metal back end of line (BEOL) processes is also critical for a successful light guide. BEOL process steps and temperatures were optimized to minimize any degradation or change in index of refraction of the light guide material. Figure 1 illustrates a cross-section of Aptina's 1.4um pixel with light guide design. (Note that the visible non-uniformity of the light guide material is due to de-processing artifacts introduced by both mechanical cleave and chemical stain.)

Aptina uses a modified n-substrate PD process for it's small pixel development described in (1, 2). Further optimization of the PD structure to reduce crosstalk and increase quantum efficiency was done by extending the depth of the PD depletion region. Figure 2 shows a simulated combined probability of photon absorption and electron collection as a function of Aptina's PD depth. As can be seen from the plot, to obtain higher collection probability and achieve >80% absorption of green light, the equivalent depth of the PD absorption box should be on the level of 2.5 – 3.0 um.

In addition to extending the PD depletion depth, the PD must also extend laterally to capture the light that spreads in the silicon which might otherwise contribute to optical cross-talk. Meeting these twin requirements while also ensuring sufficient electrical isolation between adjacent pixels poses challenges to processing and implant engineering. PD and isolation implants and their location in the process flow were optimized for Aptina's advanced low thermal budget logic process.

Aptina's light guide has been optimized taking into consideration how light propagates through both the stack of layers above the Si, and in the Si itself. The goal was to maximize the amount of light reaching the PD and staying within the Si PD absorption box. This optimization was done for incident light with zero chief ray angle (CRA) for pixels located at the center of the array, as well as for incident light with larger CRA for pixels located at the edge of the array. Figure 3 presents results of FDTD simulations of 600nm light propagation for a 1.4um pixel with F number 1.4. The simulations compare (a.) a pixel with a light guide illuminated with a CRA=0 of incident light, vs. (b.) a pixel with a light guide and shifted ulens/CF for CRA=45 degrees of incident light, vs. (c.) a pixel with no light guide. In all cases, the dashed line rectan-

gle depicts an equivalent absorption box of the PD. Absorption of the Si is artificially zeroed to allow better view of light propagation through the Si. All other optical properties of the Si and layers above the Si were not modified. As can be seen from the simulations, significant scattering of light within the Si is observed when no light guide is present. With proper adjustment of the light guide design, we can first maximize delivery of light to the PD surface, and second achieve the situation where light stays within the PD absorption box for both normal incidence and high angles (CRA) of light;

The last observation is most important: Aptina's light guide technology serves as a tool to straighten light, direct it towards the PD, and create the condition where light remains within the absorption box of the Si PD. The combined effect of an optimized light guide and extended PD depth results in up to a 50% increase in Quantum efficiency and 30% reduction in crosstalk for a front side illuminated 1.4um pixel.

2. Pixel Design and Pixel Array Architecture

Aptina continues exploring new pixel architectures that benefit small pixel development. We will consider several pixel architectures with a reduced amount of pixel components that allow effective pixel shrinks.

Pixel with "Internal Reset Control" (IRC). A conventional CMOS image sensor with a 4T-pixel has row drivers to control the voltage on the gate of the reset transistor as well as metal routing within the pixel array that connect the reset gates with corresponding row drivers. An IRC pixel eliminates the need for the reset metal routing and respective row drivers by connecting the reset gate inside the pixel to the pixel output line. By using new timing, the pixel output line can be used to reset the floating diffusion, and thereby maintain proper operation and performance of the 4T pixel. The schematic of an IRC pixel is shown in Figure 4a. Detailed descriptions of pixel operation and timing diagram can be found in (2, 3). In addition to improving fill factor and simplifying readout circuitry, the IRC pixel allows shorter readout time which becomes more critical for large pixel arrays (8–10 Mpix and larger) combined with HD video modes. The IRC pixel architecture has been successfully implemented on many of Aptina's products with 2.2um, 1.75um, and 1.4um pixels.

Pixel with "Internal Reset Control and No Row Select transistor" (IRCNRS). This pixel architecture is similar to the IRC pixel, but allows elimination of the row select transistor. This pixel originated from the basic idea described in (4) but was modified for the 4-way CEPA. The schematic of the IRCNRS pixel is presented in the Figure 4b. This pixel was successfully demonstrated and will be used in future Aptina products.

Pixel with No Row-Select transistor and shared TX/RST control. In this pixel design we have used another approach to increase fill factor and metal opening for super small pixels - using a pixel architecture with no row select transistor and the same metal line for TX and RST control of pixels located in adjacent rows. The schematic of the pixel is shown in Figure 4c. The RST gate of the pixel in row (n) is connected to the TX gate of the pixel in row (n-1). As a result, there is no need for a TX line routed within the pixel array, which significantly simplifies pixel layout, reduces pixel routing, and increases the pixel optical fill factor. Aptina first introduced the pixel with shared TX/RST about a year ago and has presented detailed pixel operation and first results from test chips in (2). At present, a modified version of this pixel architecture has been implemented into one of Aptina's newer 1.75um products. Because of the non-shared FD in this pixel architecture, and an advanced pixel layout, we were able to boost conversion gain of the FD to a record number of 300uV/e. Responsivity on the latest revision of the pixel reached 2.0V/lux*s, and sensor readout noise was reduced to less than 1e. As a result, this 1.75um pixel demonstrates significantly enhanced low light performance comparable to our best 2.2um pixel products.

3. 1.4um pixel characteristics & image quality of sensors with ¼" optical format

Many of the process and architecture enhancements mentioned above were implemented into the first of Aptina's 1.4um pixel family of products – a 5Mpix SOC with ¼" optical format. A summary of the pixel characteristics is presented in Table 1, and the spectral QE plot is presented in Figure 5. The pixel achieves high quantum efficiency, small crosstalk, and high image quality in a ¼" optical format Image sensor.

Continuing consideration of Image Quality in Equal Optical Format described in (6) Figure 6 presents a relative SNR10 metric normalized per pixel area for Aptina's pixels and pixel generations. As can be seen from the plot, the 3rd generation of Aptina's 1.4um pixel reaches "scaled" performances compared to the best and well known Aptina's products with a larger pixel size. Figure 7 compare images from the full line of Aptina mobile products with ¼" optical format, starting from the first VGA product with a 5.6um pixel size, through 1Mpix (2.8um), 2Mpix (2.2um), 3Mpix (1.75um), and latest addition of 5Mpix product with a 1.4um pixel size. Images are taken with f/2.8 lens, at 100 lux and 66.7ms integration time. Zoomed fragments preserve equal optical format. As can be seen from Figures 7a and 7b, image quality from a SNR standpoint is very similar with the added benefit of higher spatial resolution for the latest 5Mpix – 1.4um pixel product.

4. Conclusion

Aptina's pixel and process innovations continue to drive small pixel development with "scaled" performance. The latest addition of Aptina's 1.4um pixel extends it's family of products with "scaled" performance, providing superior image quality compared to previous generations of products of the same optical format, with the added benefit of higher spatial resolution.

5. Acknowledgements

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6. References

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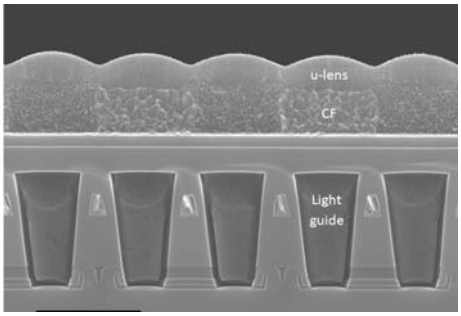

Figure 1. Cross-section image of Aptina's 1.4um pixel with light guide

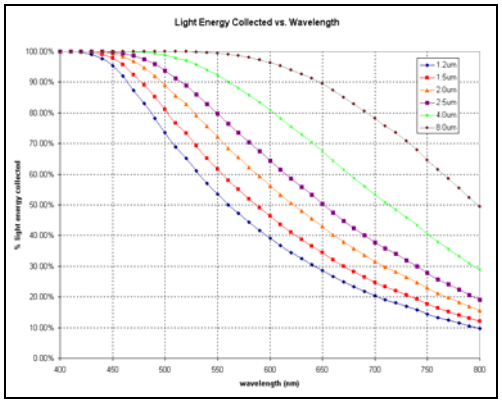

Figure 2. Combined probability of photon absorption and electron collection for different equivalent absorption depths of the PD

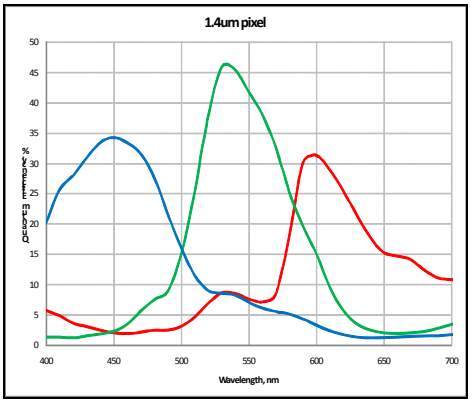

Figure 5. Quantum Efficiency Spectral plot for 1.4um pixel

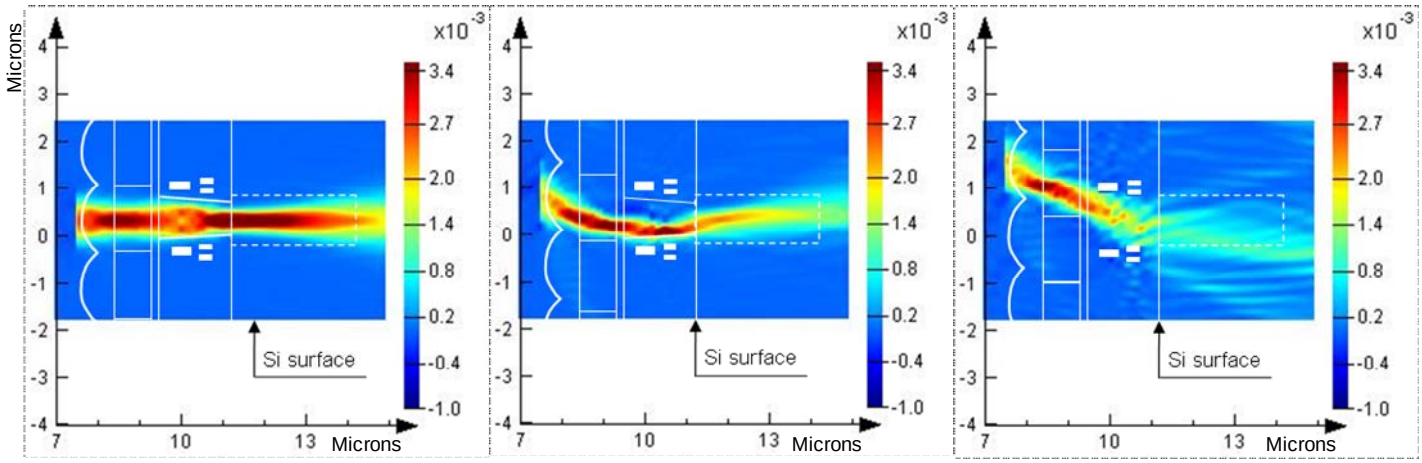

Figure 3. Examples of light propagation FDTD simulation for 1.4um pixel for 600nm wavelength, F number 1.4, and different CRA of incident light.
a. – pixel with light guide, CRA of incident light is equal to zero;
b. – pixel with light guide and shifted ulens/CF, large CRA of incident light;
c. – pixel with shifted ulens/CF and no light guide, large CRA of incident light.

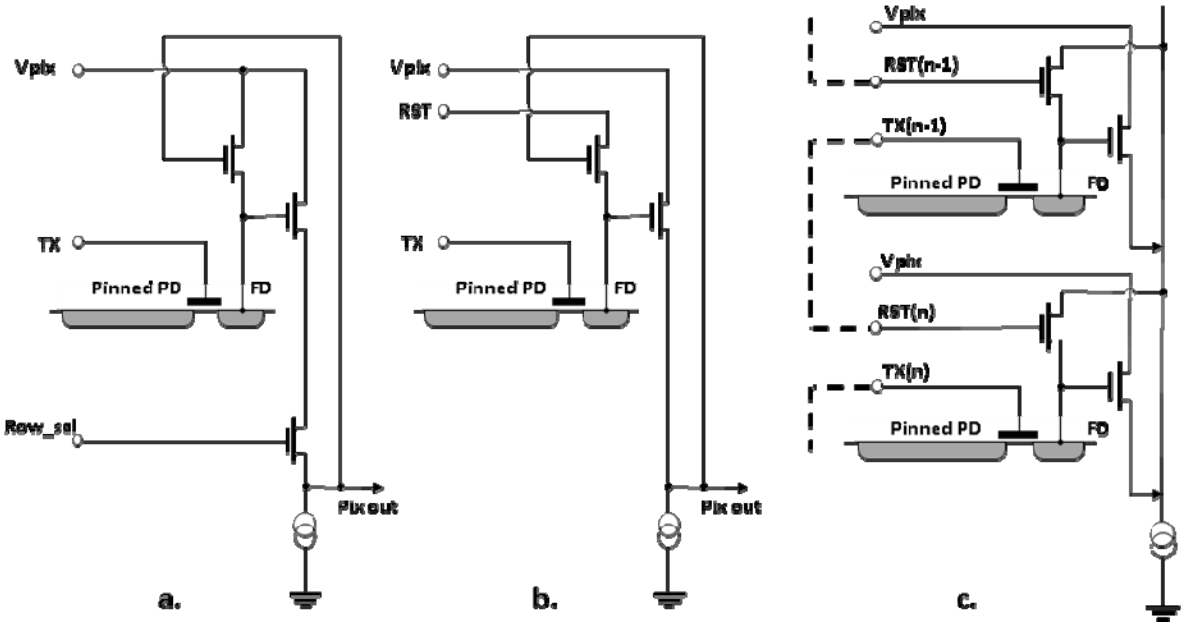

Figure 4. Pixel architectures for small pixel development
a. – pixel with Internal Reset Control (IRC)
b. – pixel with Internal Reset Control and No Row Select transistor (IRCNRS)
c. – pixel with no row select transistor and shared TX/RST control

Table 1

Conversion gain (uV/e-)	190
Pixel capacity - linear range (ke-)	5.0
Read noise (e-)	1.6
Pixel dynamic range (dB)	70
Dark current @60C (e-/sec)	< 30
Responsivity - FD (V/lux-s)	0.8
Measured SNR10 (module lens f/2.8, 15 FPS 18% scene reflectance, after applying CCM)	120

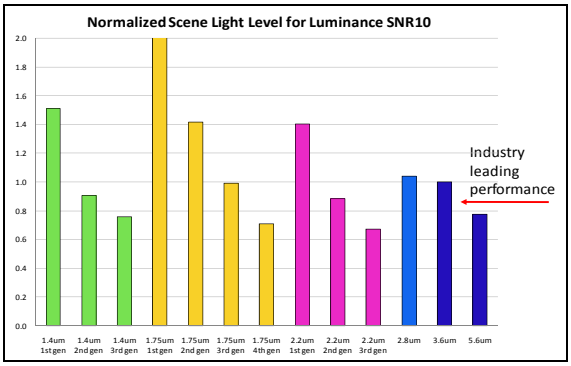

Figure 6. Normalized SNR10 after CCM for Aptina's pixels

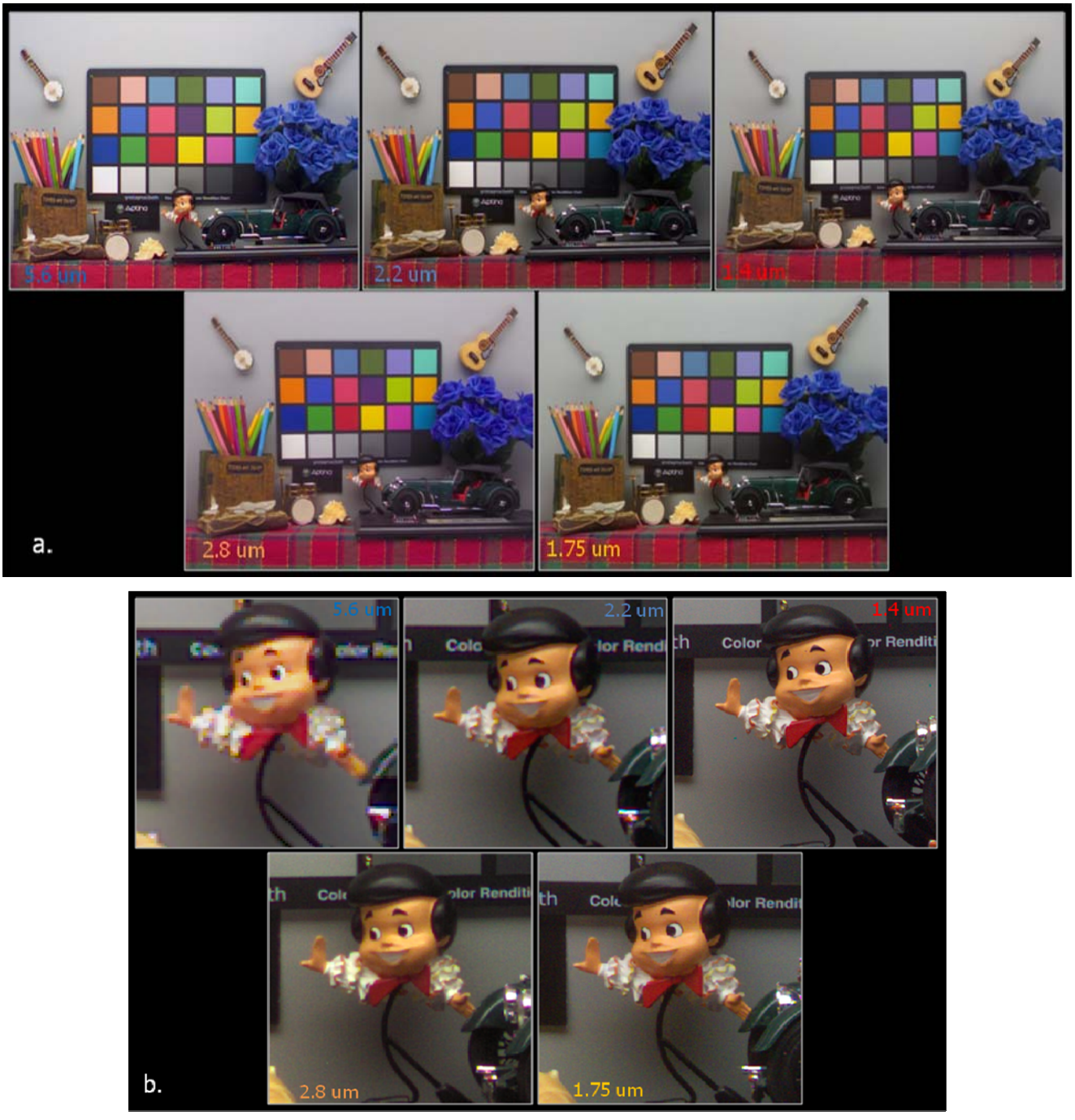

Figure 7. Image comparison for Aptina's SOC for applications with for 1/4" optical format: VGA-5.6um pixel, 1Mpix-2.8um, 2Mpix-2.2um, 3Mpix-1.75um, and 5Mpix-1.4um pixel.