A 1.4 μm pixel front-side-illuminated image sensor for mobile phones

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A first-generation front-side-illuminated 5-Mpixel, ¼"-format image sensor built in a 0.11 μm CMOS process with 1.4 μm pixels is presented. It has a state-of-the-art 1.4 μm pixel with the performance required for mobile operation. This is achieved by the use of disruptive technologies in order to obtain optical response, charge capacity, noise, and uniformity. The resulting image sensor achieves an SNR of 10 at 70 lux, a well capacity of 5500 h^+, lag < 1, and a dark current of 30 pA/cm^2 at 60 °C. The chip has an effective pixel array of 3,248 (H) × 1,556 (V) that can be read out through either a 96 MHz parallel or a high-speed MIPI interface and that can achieve 720 p operation of 60 fps.

The primary challenge for an array with a pixel of this small size is obtaining good signal-to-noise at the lowest light level. Pixel and microlens designs are optimized to maximize fill factor and angular acceptance while controlling optical cross-talk. Sensitivity is increased through the incorporation of a CFA pattern that has 50% clear pixels and a 4 × 4 pixel repeat tile. It is found that below 1.60 μm pixel size, there arises the need for aggressive processes and design rules in conjunction with pixel design to overcome diffraction-limited apertures and that electromagnetic modeling is crucial for the design of the CFA and the optical stack. For example, it is used to address the challenge presented by a low profile module through multilayer easing including the microlens, the color filter, and the metal interconnects.

A related challenge is building a pixel with maximized photodiode area for charge integration, with high conversion gain to lift the signal above the electronic noise without significant lag and with minimum dark current and bright defects. This is achieved by building in a pMOS pixel process integrated into a conventional 0.13 μm logic process technology [1] and by systematically pushing design rules. The photodiode area is maximized through operation that does not require a select transistor and that used 2 × 2 sharing of pixel transistors.

The imaging array layout, the pixel architecture, and the color filter pattern combine to enable multiple modes of operation including full-resolution still photography and video modes based on decimation and binning of the color and the clear pixels to cover a broad range of illumination levels while maximizing image brightness and minimizing color aliasing.

Ref [1] E. Stevens, et al., “Low-crosstalk and low-dark-current CMOS image-sensor technology using a hole-based detector”, Digest of 2008 IEEE ISSCC, 61-62 [2008]

Table 1: Video modes of operation (quarter-resolution)

mode	2 × 2 readout	Data rate	Comments
Bayer	R+R, G+G, B+B	60 fps	Standard Bayer readout using color pixels
Bayer +1	R+R+P, G+G+P, B+B+P	60 fps	Desaturated Bayer readout for low light
Bayer +2	R+R+2P, G+G+2P, B+B+2P	60 fps	Desaturated Bayer readout for lower light
“Mode 5”	R+R & P+P, G+G & P+P, B+B & P+P	30 fps	Trade data rate for increased sensitivity & saturation

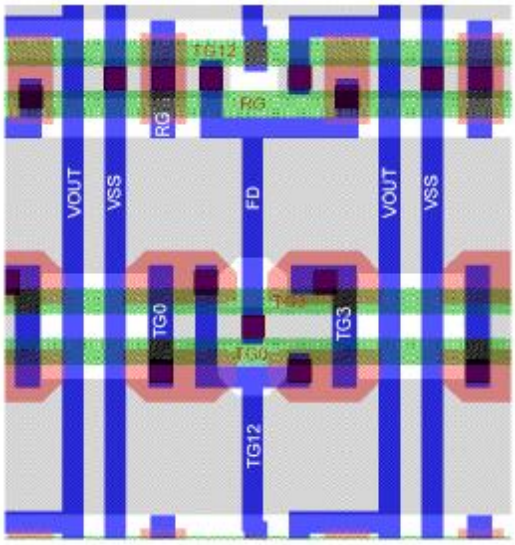

Figure 1: Pixel with metal layout

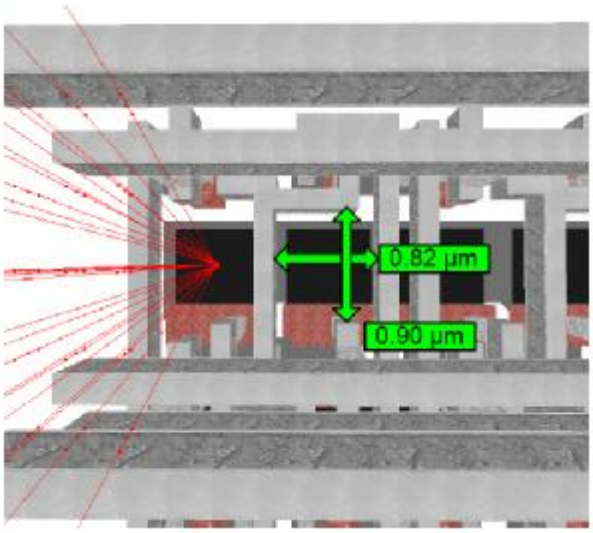

Figure 2: Photon view of pixel

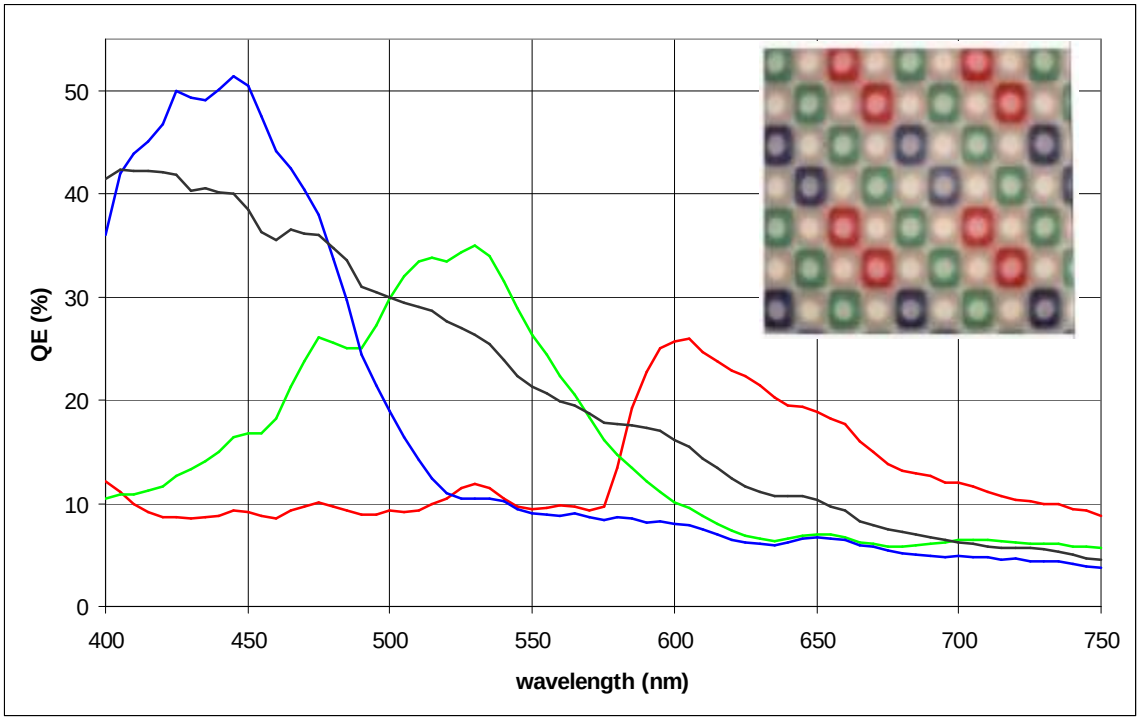

Figure 3: QE (blue, green, red, clear) & Sparse CFA pattern (insert)

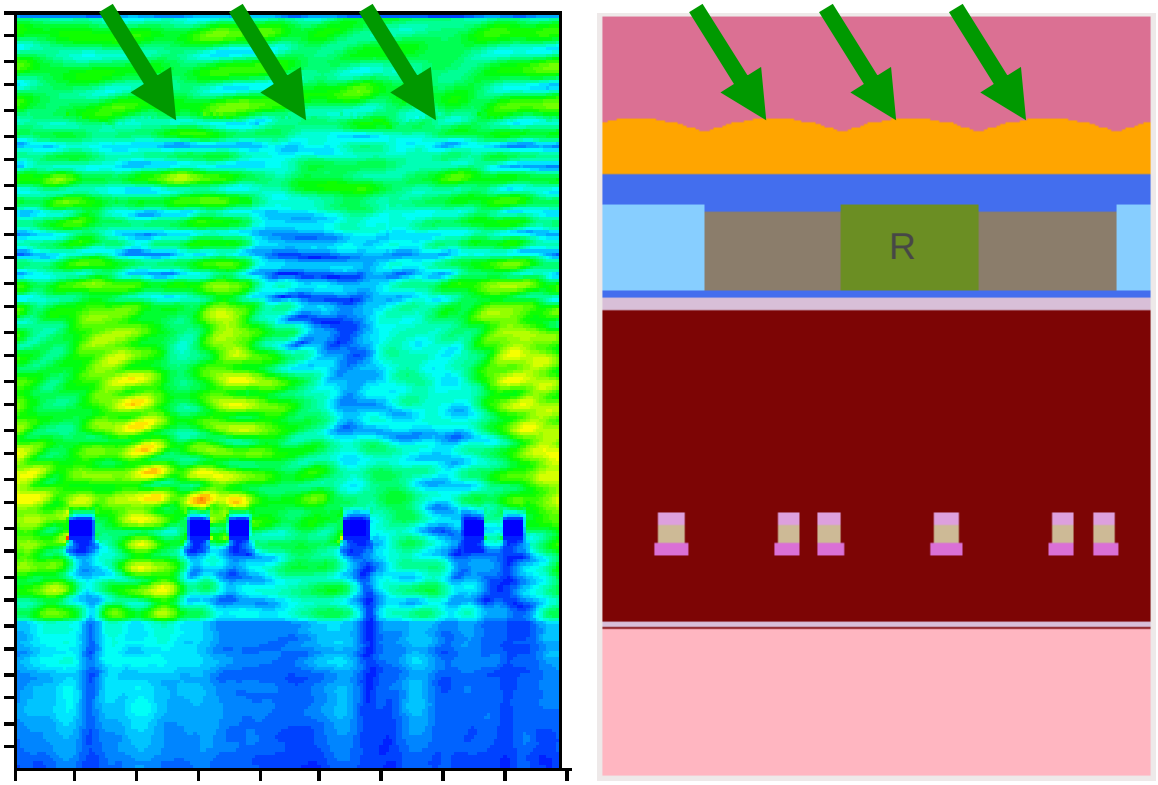

Figure 4: EM example showing easing: EM intensity; structure

Figure 5: Image