New Integration Technology of Small-Pixel CIS with High Sensitivity

Seounghyun Kim, Taegyu Kim, Munhwan Kim, Dongbin Park, Heesung Shim, Jongtaek Hwang, Sungho Jun, Ohjin Jung, Joonku Yoon, Minhyung Lee, Chulho Park, Jaewon Han, Joon Hwang

CIS Process Development Team, Mixed Foundry Division, Dongbu HiTek Co., Ltd.
474-1 Sangwoo-Ri, Gamgok-Myeon, Eumseong-Gun, Chungbuk, 369-852, Korea
E-mail: seounghyun.kim@dongbu.com Tel: +82-43-879-6975 Fax: +82-43-879-9902

Abstract

We have developed the new pixel structure using the wafer to wafer bonding and the cleaving technologies, by which we can maximize photodiode area. The new technology consists of 4 steps; (1) Logic wafer integration, (2) Top photodiode integration, (3) wafer bonding and cleaving, (4) process after cleaving. As the results, we obtained a good image quality despite of small pixel as well as reduce the chip size, because the new structure has no metal levels issue. Although we got the good results more than expected, we should optimize the top photodiode doping conditions and improve bonding quality.

1. Introduction

CMOS Image Sensor has experienced a high volume increase for several years. Continuous pixel shrink has been created due to the strong demand for smaller chip size and high resolution of CMOS Image Sensor [1-3]. However, smaller pixel CIS typically leads to the degradation of image quality and reduction of pixel sensitivity. Therefore, many researchers have focused on the development of new integrated scheme of CIS such as Backside-Illuminated and 3-D integrated image sensor for small-pixel CIS [4-7]. However these technologies use difficult integration methods such as Backgrinding and TSV (Through Silicon Via). They also need high cost and have difficulty of the mass production. In this work, we have developed the new CMOS Image Senor with 1.3M resolution of 2.2um pixel using the wafer to wafer bonding and the cleaving technology similar to the SOI wafer fabrication method [8-12]. By using this technology, we obtained a possibility to apply to mass products at a low price

2. Pixel Structure and Advantages of New Integration Technology

Fig. 1 shows the schematic diagram of the new integration. Photodiodes and pixel operation circuits are located in the top Si region and the bottom Si substrate, respectively. Therefore the new structure maximizes the photodiode area. Finally, it can get higher sensitive and better pixel performance than the conventional pixel structure. And also it dose not need micro lens, because photodiodes are located in the top region. The new structure has no metal levels issue. That means it can reduce the chip size. Fig. 2 shows the cross-sectional image of the new structure. From the result of SEM image, we can confirm the new pixel structure using the wafer to wafer bonding and the cleaving technologies.

3. New Process Integration for High Sensitivity

The new technology consists of 4 steps as below;

(1) Logic wafer integration
(2) Top photodiode wafer integration
(3) Wafer bonding and cleaving
(4) Process after cleaving

3. 1 Logic wafer integration

In the logic wafer integration, we included pixel operation, ISP, CDS, ADC and analog circuits. BEOL is conducted by the general Al processes such as metal wiring, IMD deposition and CMP (Chemical Mechanical Polishing), as shown in

Fig. 3. Additional metal lines are also fabricated for connecting the top photodiode with the pixel operation circuits. In order to obtain good bonding with the top photodiode wafer, the RMS roughness of final IMD surface needs below 5Å for 2um x 2um area. By using this technology, we can also make the logic wafer, which has more than 4 metal levels for chip size reduction.

3. 2 Top P/D Wafer integration

As shown in Fig. 4, after the screen oxide was deposited on the Si wafer, n type and p type ions were implanted to make photodiode and ohmic contact. And then the wafer was annealed by the RTP (Rapid Thermal Process) for ion activation. The wafer was exposed to hydrogen implantation with dose of 1E16 - 1E17/cm^2 after photodiode formation. The trapped hydrogen atoms combine with silicon atoms to form Si-H bonds. During hydrogen implantation at room temperature, the elastic strain energy induced by residual stress plays a predominant role in fracture of Si-Si bonds. And also the high temperature annealing makes significant contributions to the fracture process [10]. A thin damaged layer appears at the depth of high hydrogen concentration near the projected range, as shown in Fig. 5. We have to determine the implantation energy considering region damaged by hydrogen ions. In this experiment, the wafer was exposed to the energy condition with projected range of about 1.3um. And then we obtained top photodiode with 1.2um thickness. Because there is damaged region of about 0.1um thickness inside the silicon, it must be removed as described in 3.3. Finally, the screen oxide is eliminated by DHF chemical.

3. 3 Wafer bonding and cleaving

The logic and top photodiode wafers were cleaned with various chemical for particle remove and surface treatment. And then both wafers underwent plasma treatment for strong bonding at low temperature. The plasma activation was carried out using O, N, Ar gases. The wafers were immediately loaded into the wafer bonder and bonded at room temperature. To achieve strong chemical bonds between the two wafers, the bonded pair was annealed at the temperature from 200℃ to 400℃ for several hours under N2 gas atmosphere. By inserting a razor blade near the bond interface of the bonded pair, a mechanically induced crack propagates throughout the H-implantation zone in the top Si wafer. The layer transfer occurred when the H-implanted region was weaker than the bonded interface. So we got the transferred silicon layer, as shown in Fig. 6. Although the thin silicon layer was transferred to the logic wafer, there were many defects in the top region of the transferred silicon. This damaged region has to be removed by CMP or chemical process for good image quality.

3. 4 Process after cleaving

After top photodiode layer transfer to the logic wafer, we have fabricated pixel to pixel isolation regions using silicon etch, oxide gap-fill and CMP process, as shown in Fig. 7. The isolation regions will be expected to improve the signal crosstalk problems between adjacent pixels. And then the ground metal lines are manufactured by metal patterning processes, which are used for forcing the potential and hole removal. Finally, the passivation layer, pad and color filter arrays are subsequently integrated (Fig. 1, Fig. 2). The new CIS dose not need micro lens, because photodiodes are located in the top region.

4. Image characteristics of the New CIS

Fig. 8 and Fig. 9 show the sampled images obtained by new integration technology. Although the work is the results of the early development, we can get good image quality more than expected. Fig. 10 represents the optical performance data of the New CIS. We evaluated the new integrated CIS under the 15 lux illumination. The black level is about 40mV. It is higher than conventional method due to the top photodiode damage induced by etch process. We need more tests for reduction and removing defects in the top photodiode region. The sensitivity and saturation are 761mV/lux sec and 565mV, respectively. It is similar level to the conventional CIS. So, more researches have to be focused on improving white characteristics. For example, we will optimize the photodiode doping conditions and thickness of top silicon layer. Most of all, we must improve the wafer to wafer

bonding quality to increase yield. The yield is currently about 10%.

5. Conclusions

For the first time, we have developed the new pixel structure using the wafer to wafer bonding and the cleaving technology. The black lever is higher than the current integration structure. And the white characteristics are similar to the conventional CIS. From this study, we obtained a possibility to apply to mass products at a low price.

6. References

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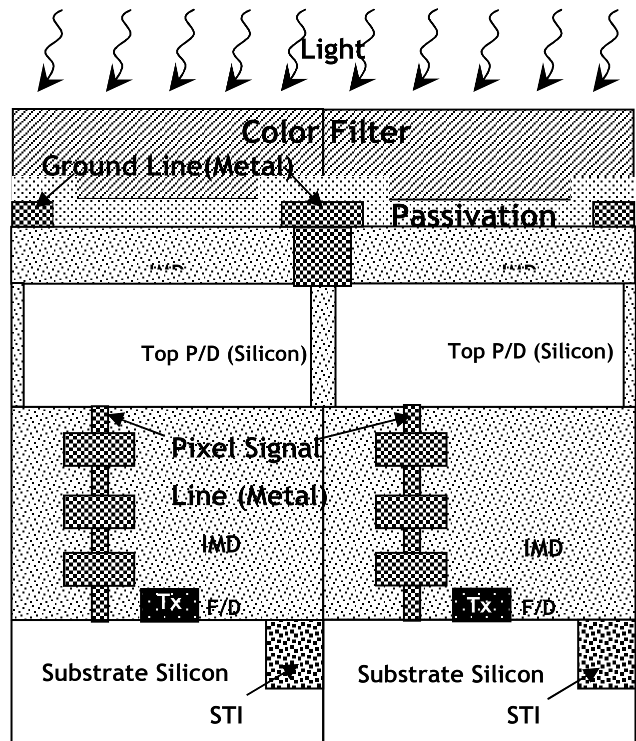

Fig. 1. Schematic diagram of new CIS

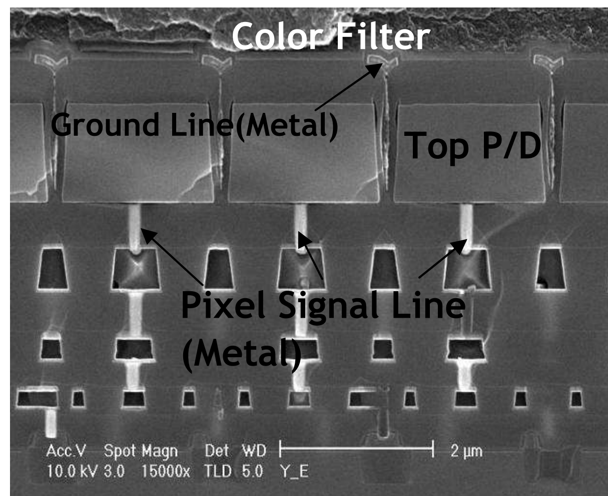

Fig. 2. Cross-sectional image of new CIS

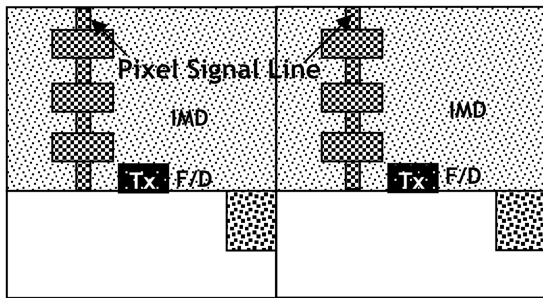

Fig. 3. Logic wafer integration

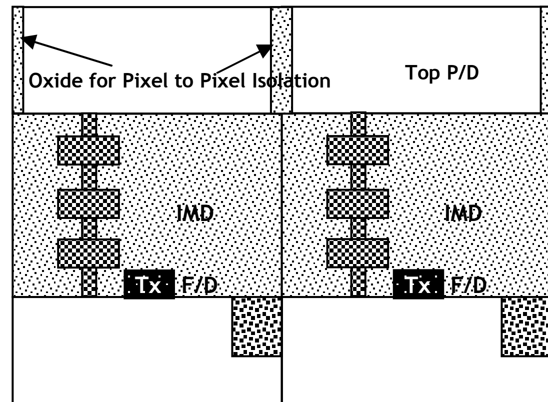

Fig. 7. Pixel to Pixel Isolation

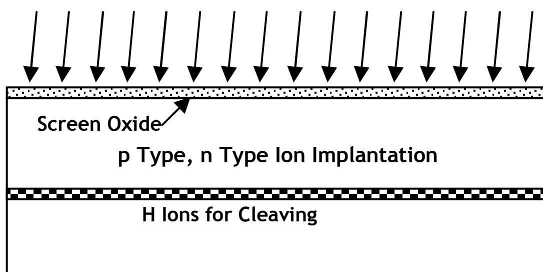

Fig. 4. Top photodiode wafer integration

Fig. 8. A captured image by new CIS

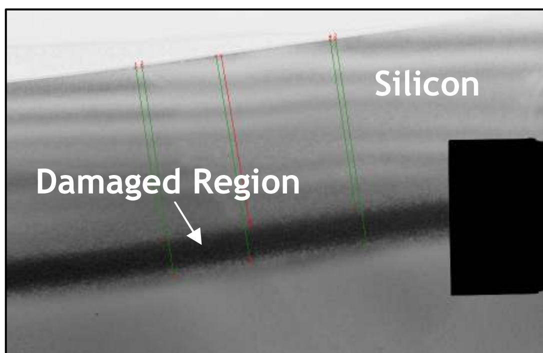

Fig. 5. TEM image after H implantation

Fig. 9. A captured image by new CIS

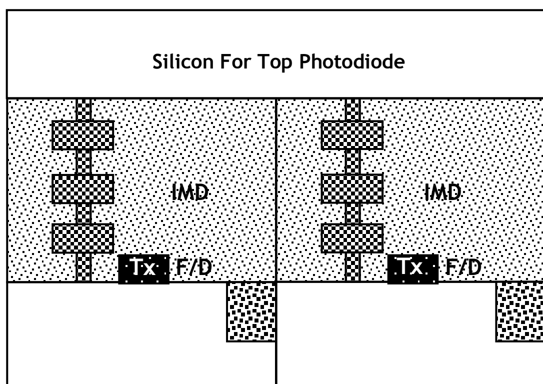

Fig. 6. Wafer to wafer bonding and cleaving

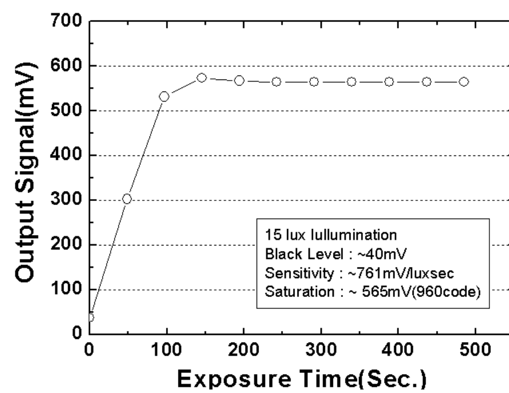

Fig. 10. The optical performance data