

CMOS Synchronous shutter backside illuminated image sensor for hyperspectral imaging

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Abstract

There is an ongoing debate about whether CMOS or CCD is the better technology for space imaging. The reality is that the answer depends on the exact application being considered. In this article we present one field, hyperspectral imaging (HSI), where CMOS technology can potentially avoid some of the disadvantages that have been seen with CCDs and discuss the design of a sensor that is optimised for this application.

The challenges with hyperspectral imaging result from the very large difference in intensity between the weakest and brightest spectral lines. The use of CMOS technology removes the frame-shift smear that can produce significant crosstalk. The design of the sensor has been focused at obtaining the optimum performance from all spectral lines by allowing flexible integration time and sensitivity.

In this paper we present the concept and design of a novel pixel and sensor architecture that achieves the difficult combination of *fully pipelined synchronous shutter* operation, in a *standard CMOS* technology (with higher resistivity and thicker epi), and which is capable of operating with maximum fill factor in *backside illumination*. The pixel is also capable of *CDS* operation.

1 Technology and pixel design

1.1 Technology choice

CDD imagers have been qualified for space environments for more than two decades[1]. As far as CMOS is concerned, a distinction between classical n-well photodiodes pixels and pinned photodiode 4T pixels has to be made. Classical n-well diodes are being used in multiple space applications as Star-trackers[2]. On the other hand 4T pixels have only just started being qualified for space usage. There has been a lot of interest in advanced photodiode processes as they usually offer submicron technologies (0.18 μm , 0.13 μm) more tolerant to radiation[3].

This hyperspectral sensor is based on an enhanced n-well photodiode pixel. The n-well capacitance is set to 12fF to maximize sensitivity without compromising linearity and full well charge. The pixel pitch is 24 μm . To optimize the MTF, substrate resistance has been chosen at 500 $\Omega\cdot\text{cm}$, in which case the depleted volumes under the photodiodes are abutting (Table 1), leading to a minimal pixel-to-pixel crosstalk.

Table 1: Depletion depth in a high resistivity epitaxial layer, as a function of substrate doping and photodiode voltage

p-type concentration	p-type resistivity	Depletion layer @0V	Depletion layer @1V	Depletion layer @2V	Depletion layer @3V
1.3e14/cm ³	100 Ωcm	2.6 μm	4.8 μm	5.2 μm	6.1 μm
2.6e13/cm ³	500 Ωcm	5.5 μm	9.0 μm	11.5 μm	13.5 μm
1.3e13/cm ³	1000 Ωcm	7.7 μm	12.6 μm	16.2 μm	19.0 μm

1.2 Backside illumination

To enhance the quantum efficiency (QE) and fill factor (FF), the epitaxial wafer is thinned down to 8 μ m and is used in back-side illuminated operation. Figure 1 shows a cross section of the pixel and the expected equipotential lines. To further optimize QE*FF, a metal mirror is added to the pixel. With such pixel, the simulated QExFF is presented in Figure 2.

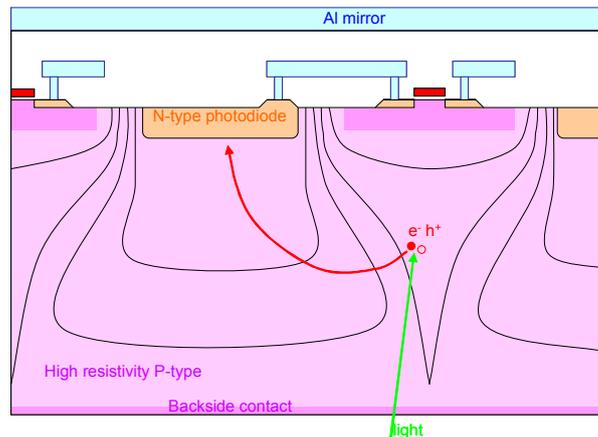


Figure 1: Cross section of thinned pixel when in a high resistivity substrate. Equipotential lines tentatively shown.

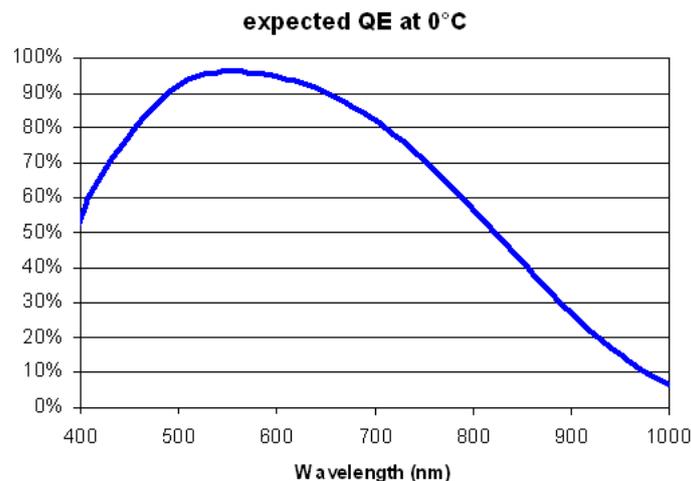


Figure 2: The HSI device's projected QE (at 0°C, for 8 μ m final thickness and 100% fill factor)

This QE curve is based on e2v's standard Backthinning process which has already been demonstrated to be effective on CMOS imagers [4]. In practice the antireflection can be optimized to suit specific project requirements.

1.3 Pixel design

The use of CMOS technology overcomes inherent limitations of frame shift smear with the classic hyperspectral imager CCDs. The pixel is designed with a fully synchronous pipelined shutter, which allows all spectral lines to be sampled at the same spatial position. Moreover the sensitivity can be programmed separately for each spectral line of the image sensor to adjust to the flux for each particular wavelength. The pixel topology is in fact quite versatile, allowing operation modes that make the sensor fit for a wider range of applications (such as spectroscopy) than hyperspectral imaging only. The imager operates in pipelined synchronous shutter mode, but can also be driven in rolling shutter mode, with or without correlated double sampling (CDS). The basic pixel schematic is presented on Figure 3.

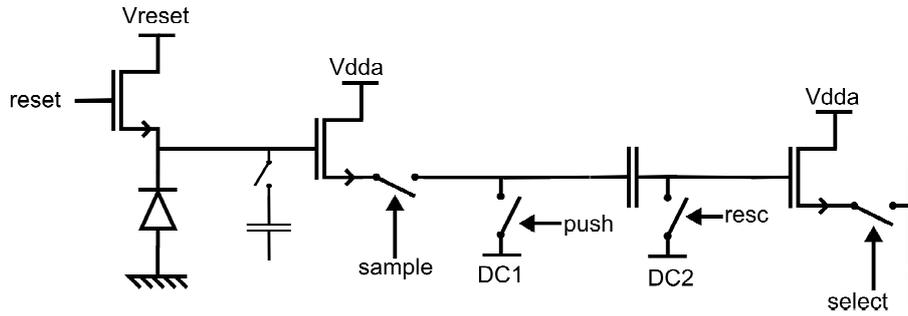


Figure 3: Pixel schematic

The DC1 reference voltage and push switch act as an in-pixel level shift. The sense node capacitance is programmable. The pixel has a full well charge of 150ke⁻ in high sensitivity mode (Figure 4), and 450ke⁻ in low sensitivity mode.

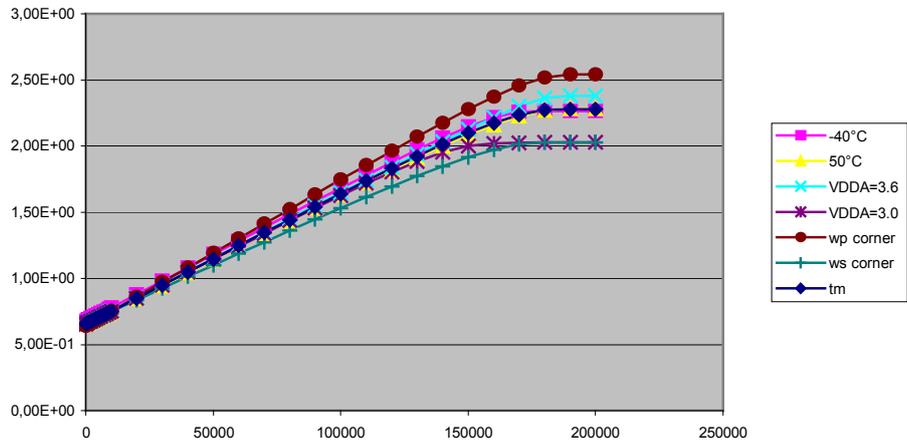


Figure 4: The pixel's charge response and full well charge for all corners, showing technology and operating conditions dependence,

The pixel layout is shown in Figure 5. MIM capacitors are used to minimize the silicon footprint of readout circuitry. The pixel has a metal mirror that is reticulated and centered on the photodiode center.

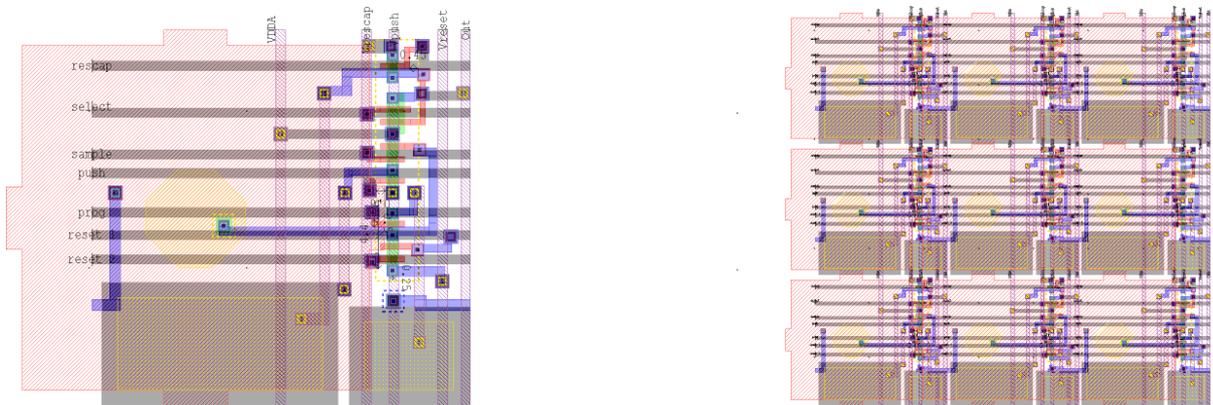


Figure 5: pixel layout (Left) and example of 3x3 arrangement (right)

2 Sensor architecture

2.1 Device specifications

The main device specifications are presented in Table 2. The large pixel number and large pixel size necessitated “stitching”. A high degree of parallelism is needed to reach a high frame rate while keeping the analog bandwidth as low as possible to limit readout noise.

Table 2: Hyperspectral imager specifications

Resolution	1024x256
Pixel pitch	24 μ m
Number of spectral bands	256
Readout speed	250 frames per second
ROI, k windowing	Random access in Y-direction (spectral direction) only
Full Well charge with 1% linearity	100ke ⁻ and 300ke ⁻ (programmable)
Conversion factor	12fF or 13 μ V/e ⁻ 36fF or 4 μ V/e ⁻
Total noise	<50 e ⁻ in basic mode without CDS <20 e ⁻ with CDS

2.2 Floorplan

The sensor floorplan is presented in Figure 6. The stitching reticle is divided into 2 sections: one peripheral block and one central (pixels array) block. The peripheral block holds the line addressing function. It is symmetric at the left and right sides of the chip. The pixel sensitivity is programmed using a shift register in the left and right peripheries.

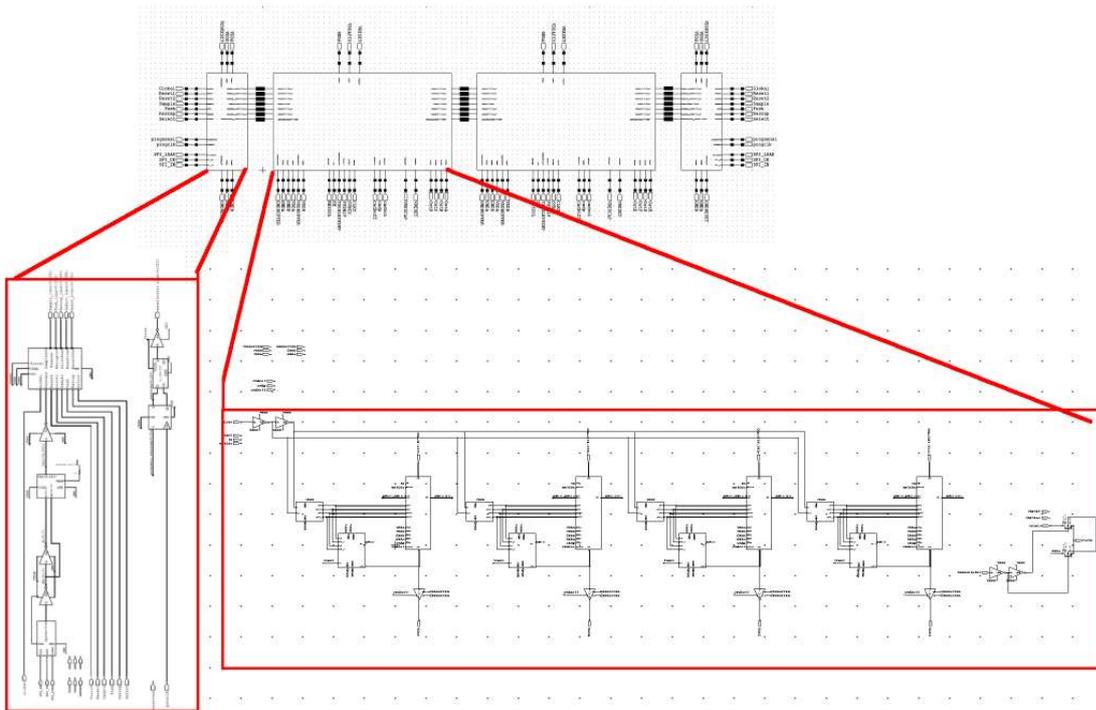


Figure 6: sensor floorplan

The central block contains 256x512 pixels and the corresponding readout structures. When repeated two times, one obtains the 1024x256 nominal arrays size. By stitching it is possible with the same reticle to achieve arrays from 256x512 to more than 256x2048 pixels. Readout is performed with a classical column sample and hold and multiple parallel analog multiplexers.

3 Conclusions and Perspectives

The device presented is the first generation of a versatile CMOS hyperspectral image sensor. Several variants of the basic operation mode are possible and are being explored. One possibility is to use a buried (also known as pinned) photodiode without the classic 4T pixel configuration. The buried photodiode has the advantage of being fully depletable and at the same time has low dark current as the P+ layer shields it from the interface generation centers.

4 References

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