

# Monolithic and Fully-Hybrid Backside Illuminated CMOS Imagers for Smart Sensing

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Backside-thinned monolithic and fully-hybrid CMOS imagers possessing excellent imaging properties have been successfully designed, fabricated and tested<sup>†</sup>. Monolithic imagers contain the photosensitive elements as well as the ROIC (Read-out IC) [1] on the same substrate as shown in Fig. 1a. Fully-hybrid imagers consist of a detector array which is produced separately and hybridized on a ROIC as shown in Fig. 1b. The pixel structures employed for these hybrid detector arrays are indicated in Fig. 2. The detector array is thinned, thus permitting efficient collection of photo-generated carriers through back illumination. In addition, optimized ARC (Anti Reflective Coating) is used to increase the QE (Quantum Efficiency), irrespective of the dielectric stack on the device front-side. With a fully-hybrid imager employing backside illumination, light loss due to reflection on metal interconnects is non-existent, and results in a 100% fill factor. Backside thinning [2] and processing has been carried out using innovative processing techniques [3] on 200 mm wafers making use of temporary carriers, which completely avoid the need for direct handling and processing of very thin (< 50  $\mu\text{m}$ ) wafers (Fig. 3). This allowed standard process tools to be used. Fully processed thinned diode arrays were flip-chipped onto the ROIC by means of a 10  $\mu\text{m}$  diameter Indium bump per pixel. Bump yield was assessed independently of other imaging properties by performing daisy chain measurements, and is found to be 99.98%. A pixel yield of 99.93% measured on a finished hybridized 1kx1k imager confirmed these results.

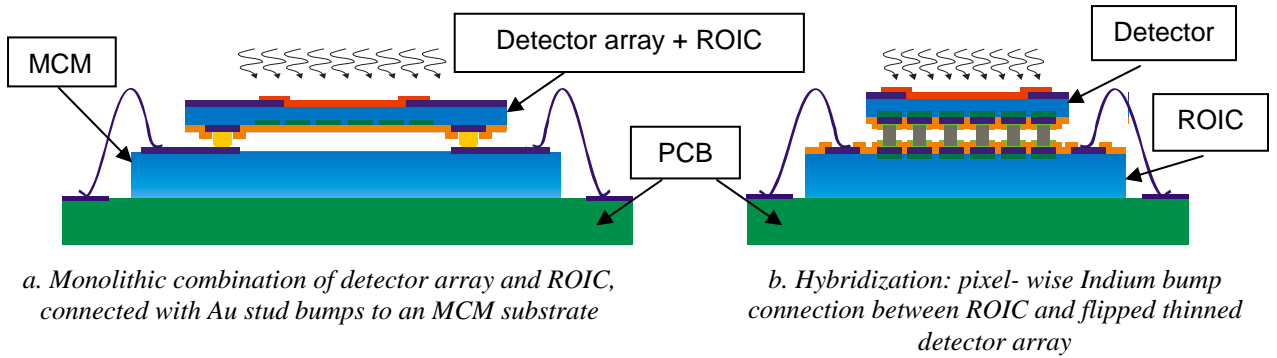
The photosensitive layer has a varying doping profile (Fig. 4) by incorporating a 50  $\mu\text{m}$  thick graded EPI layer [4]. The gradient creates a built-in electric field pulling generated carriers from the non-depleted substrate. Work is underway to further tailor this layer in order to improve the crosstalk performance.

Pictures of a completed sensor assembly are shown in Fig. 6, and a raw test image in Fig. 7. Both hybrid and monolithic imagers exhibit excellent QE (Fig. 8) after backside passivation (low-energy Boron implant and laser anneal) and ARC (Anti-reflective Coating). In addition, these imagers were measured to be sensitive to extreme ultra violet (EUV) as shown in Fig. 9. Some of the hybrid imagers have an additional crosstalk reduction measure: highly doped poly-Silicon filled high aspect ratio trenches (Fig. 2b) [5]. These 1  $\mu\text{m}$  wide 50  $\mu\text{m}$  deep trenches enforce a lateral drift field between pixels (Fig. 5), which counteract diffusion and drastically reduce electrical crosstalk. The combination of graded EPI and crosstalk reducing trenches makes these backside illuminated CMOS imagers unique. Sensors with trenches reveal excellent cross-talk performance (Fig. 10), but currently suffer from a reduced QE.

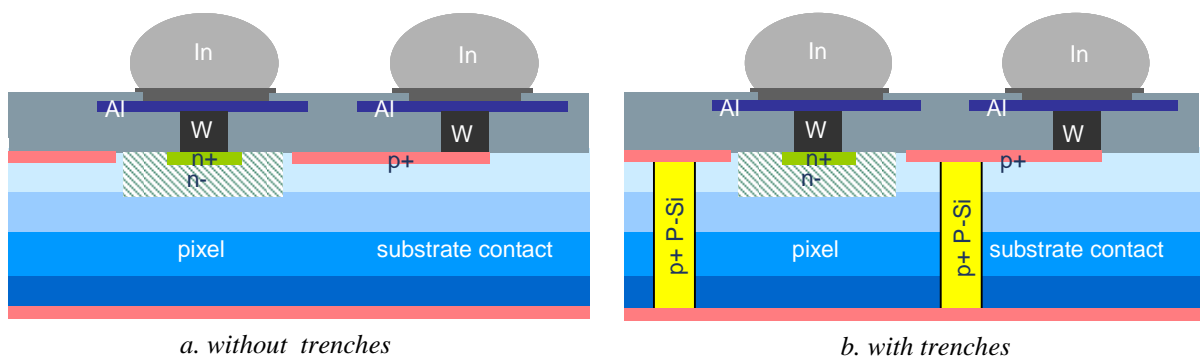
These high fill-factor sensors will further be advanced into multi-layer 3D integrated systems using the 3D technology that has been developed at IMEC (Fig. 11). Such “smart” sensors will be realized as a complete system-on-chip (SOC) including signal processing capabilities, for a whole range of complex imaging applications. Moreover, due to its peculiar pixel design that makes it sensitive outside the normal visible spectrum, they can as well be utilized for applications that demand EUV and UV.

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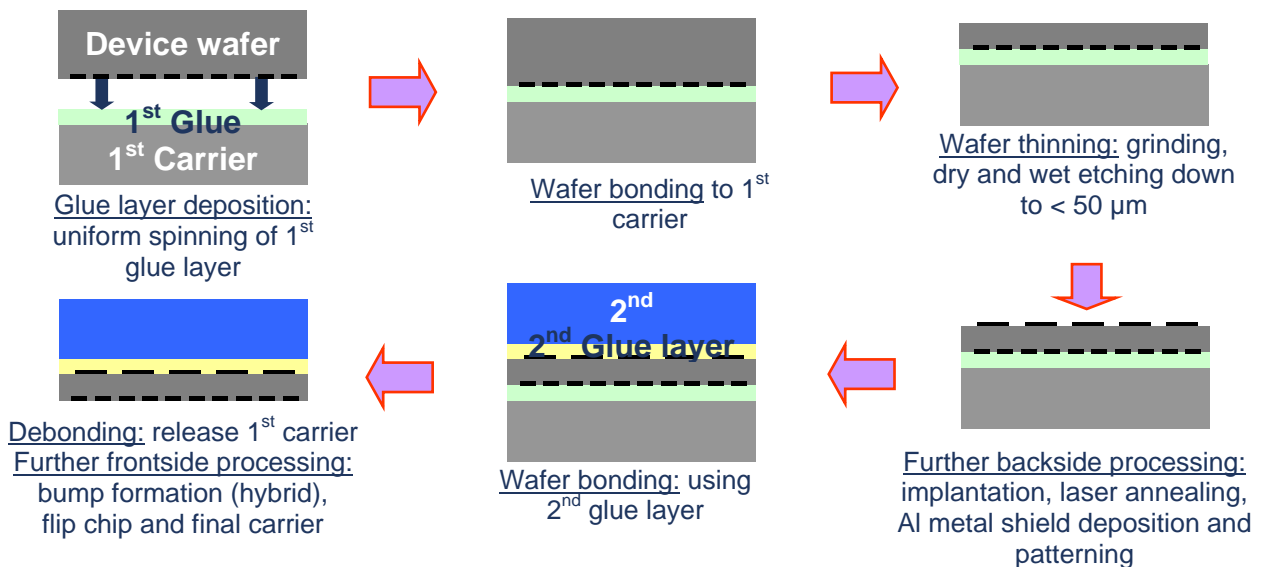
<sup>†</sup> Development of these imagers was done in the frame of an ESA funded project (AO/1-3970/02/NL/EC).



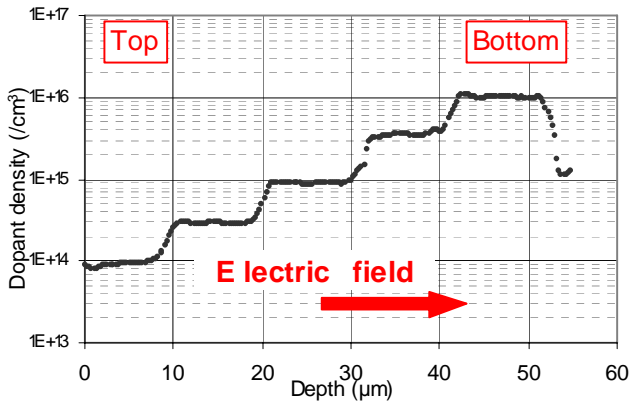
**Fig. 1:** Conceptual drawings of monolithic and fully hybridized imagers



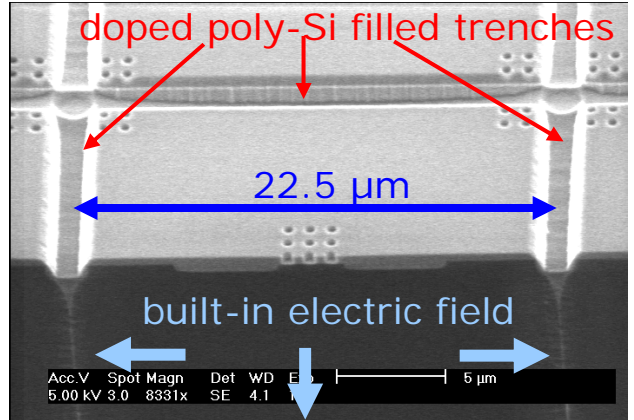
**Fig. 2:** Schematic cross-section of a hybrid detector pixel



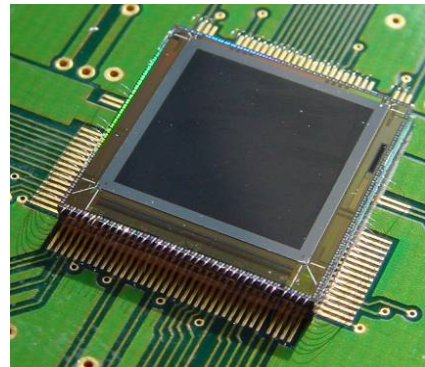
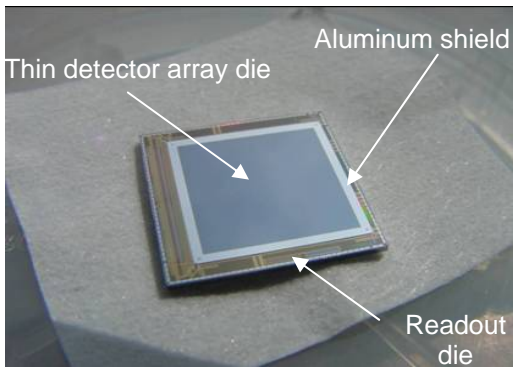
**Fig. 3:** Processing of the thin device wafers



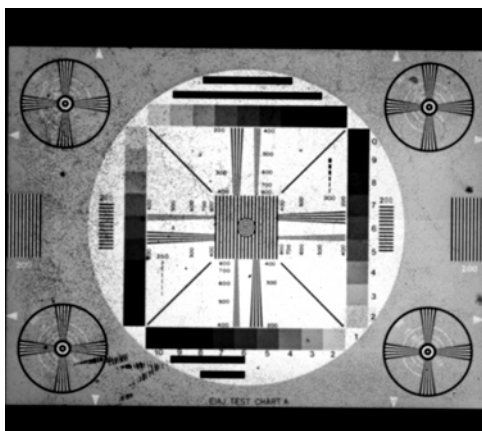
**Fig. 4:** A graded EPI profile creates a built-in electric field (opposite to minority carrier flow)



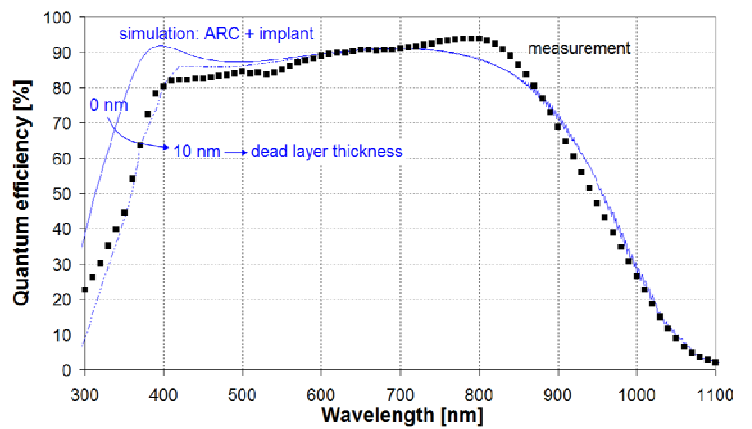
**Fig. 5:** Top view and cross section of one 22.5μm pixel surrounded by trenches (enhanced to show contrast)



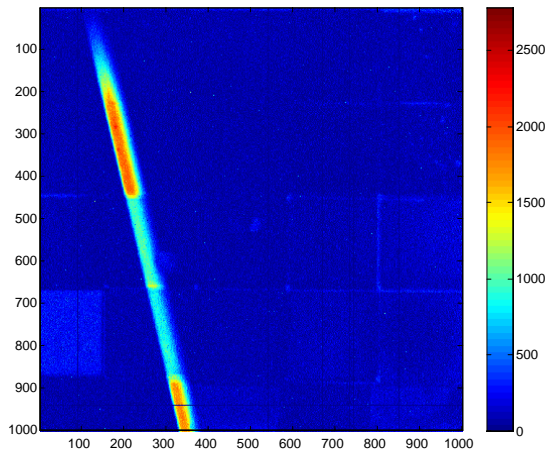
**Fig. 6:** Pictures of completed hybrid sensor (left) and mounted on a PCB (right)



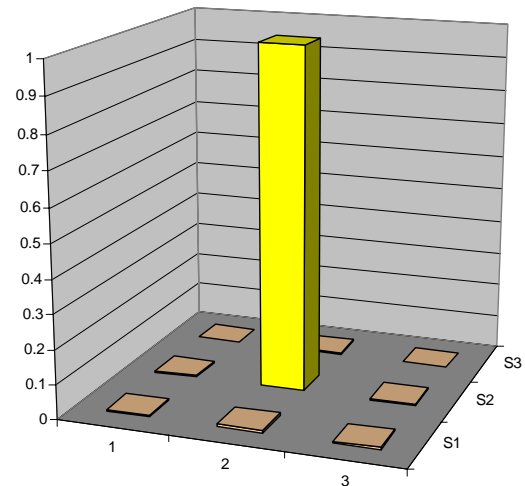
**Fig. 7:** Hybridized 1kx1k imager raw test image



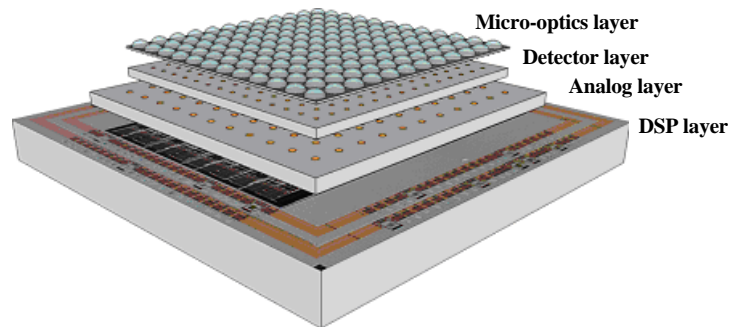
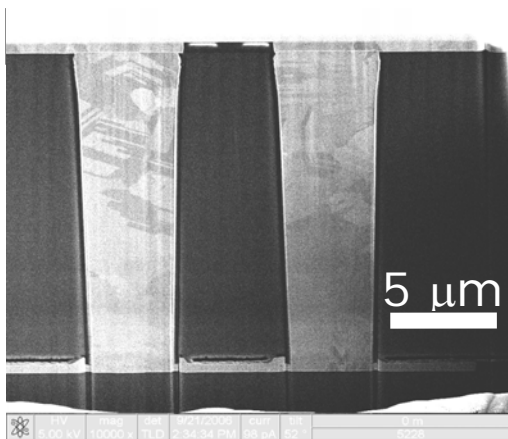
**Fig. 8:** Measured and simulated QE after backside passivation and ARC



**Fig. 9:** (False color) image made under exposure with a slit shaped beam of extreme ultra violet (EUV; wavelength = 31 nm). Non-uniformities in response are due to deliberate spatial difference in annealing conditions  
*Optical test-bench courtesy of: Ludovic Duvet, ESA, NL*



**Fig. 10:** Measured cross-talk of the trench hybrid 1kx1k imager normalized to the center pixel signal shows excellent results



**Fig. 11:** Through-Si vias realized at IMEC (left) and advanced 3D-stacked imager concept (right). Multiple layers of circuitry (digital and analog) as well as micro-optics will render a highly efficient system-on-chip (SOC) solution for imaging

## References

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- [5] K. Minoglou et al., "Reduction of Electrical Crosstalk in Hybrid Backside Illuminated CMOS Imagers using Deep Trench Isolation", *IITC Conf.*, pp. 129-131, 2008.