Towards a Three-Dimensional Back-Illuminated Miniaturized CMOS Pixel Technology using 100nm Inter-Layer Contacts

Perceval Coudrain[123], Pierre Magnan[1], Perrine Batude[3], Xavier Gagnard[2], Cedric Leyris[2], Linda Depoyan[2], Maud Vinet[3], Yvon Cazaux[3], Benoît Giffard[3], Pascal Ancey[2]

[1]*Université de Toulouse, Institut Supérieur de l'Aéronautique et de l'Espace, Toulouse, France*
[2]*STMicroelectronics, 850 rue Jean Monnet, 38926 Crolles, France, e-mail: perceval.coudrain@st.com, tel: +33-4-3892-2776*
[3]*CEA Leti-MINATEC, Grenoble, France.*

I. Introduction

Extensive miniaturization of CMOS pixels has come with challenges to preserve the electro-optical performances. Solutions have been found to enhance the Quantum Efficiency [1] [2] and reduce the noise sources, but surface-scaled photodiodes still limit the Full Well capacity and, in turn, SNR and Dynamic Range. We investigate a 3D configuration capable of simultaneous QE and Full Well enhancements, by means of a backside illumination of the pinned photodiode and the stacking of readout transistors on a top dedicated layer [3]. The increase of the photodiode area reaches 44% for 1.4μm pixels (Fig. 1).

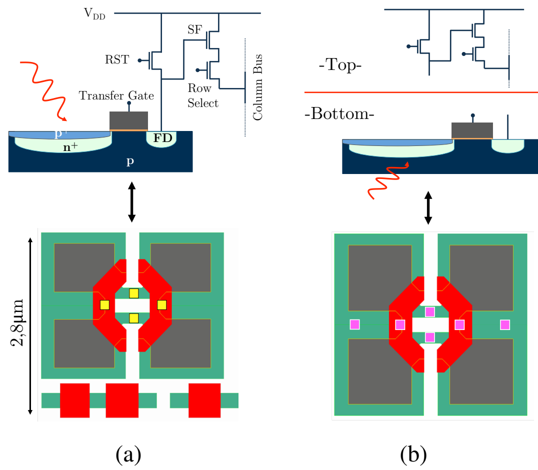

Fig. 1. Schematic and layout (bottom) of 4T 1.4μm pixels showing active (green), photodiode (grey) and poly (red) layers. a) 2D pixels with standard contacts (yellow). b) 3D pixels: back-illuminated pinned photodiode and Transfer Gate are located apart from the readout transistors, inter-layer connection is achieved by *3D contacts* (pink). The photodiode area is increased by 35%.

II. Dimensional constraints

3D pixels with relatively large pitch have been successfully reported [4] [5], but the case of highly miniaturized low noise pixels remains a technological challenge, mostly centered on the scaling of the so-called *3D vias* that connects both layers (Fig. 2).

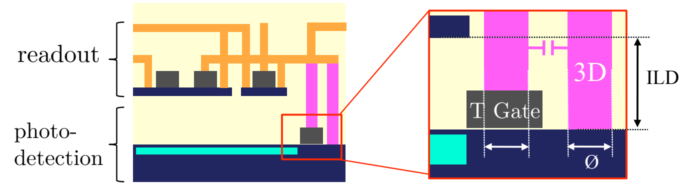

Fig. 2. 3D pixel cross-section with the so-called *3D contacts* (pink). Scaling challenges are symbolized with a zoom on the bottom layer: the diameter (⊘) of 3D contacts influences the Fill Factor, whereas their height also impact the interconnect capacitance.

The dimensions of the 3D contact contribute to the interconnect capacitance and tall contacts tend to lower the conversion factor, running counter to miniaturization needs. Moreover, the increase of the photodiode area is limited by the overall dimensions of the 3D contact on the sensing node and the transfer gate, mostly controlled by its diameter and overlay margins. Design simulations have been performed to evaluate their impact on the photodiode area of a 1.4μm pixel, as illustrated in Fig. 3 and Fig. 4. Both parameters show strong impact and the perspective of surface increase is even lost for a contact diameter larger than 0.45μm and an alignment precision higher than 0.2μm.

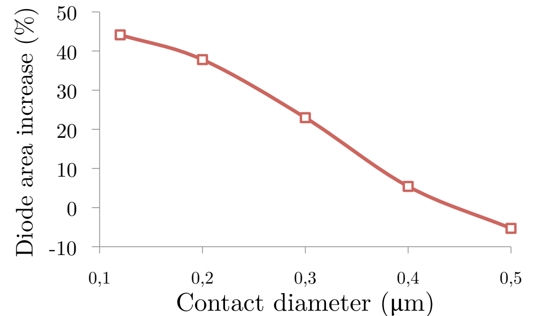

Fig. 3. Photodiode area as a function of 3D contact diameter, other design rules being keeped constants.

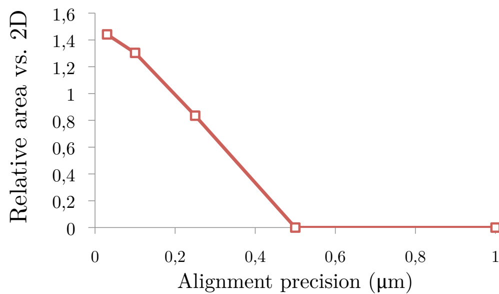

Fig. 4. Photodiode area as a function of the alignment precision for a via diameter of 0.12 μm.

Reasonable contact diameters can still be achieved by a reduced InterLayer Dielecric (ILD) thickness and a high aspect ratio etching process. However, an optimum benefit of the two-layers structure implies that the overlay margins, relative to layer-to-layer alignment [6], stay in the order of those in 2D technologies. State-of-the-art wafer bonding capabilities being known to provide minimum layer-to-layer overlays of 0.3μm (3σ) [7], the stacking of individually processed layers is hopeless to achieve the agressive design rules mandatory for a miniaturized pixel.

III. Sequential 3D construction

We propose to overcome this limitation by using a sequential integration (Fig. 5), where top layer FDSOI transistors are fabricated after processing an SOI film above the pinned photodiode and the ILD. 3D contacts, Cu metallization and process steps for Backside Illumination [1] are finally done.

The transferred SOI is transparent enough in the visible range and allows an accurate alignment of top layer lithography levels. Top contact lithography aligned on bottom gates leads to a maximum overlay of 32nm (I), in line with 2D pecifications. A thin ILD thickness further improves the alignment capabiity.

TABLE I
Top contact lihtography aligned on bottom gate

	ILD 400nm (this work)				ILD 165nm [8]
overlay	$\overline{X}$	σ	Max	Min	σ
X (nm)	1	22	32	-32	7
Y (nm)	-0.3	10	12	-13	7

Consequently, the 3D contact minimum diameter hinges upon etching capabilities. The etching of dense contacts through a 800nm SiO_2 layer, corresponding to twice the thickness of the PMD on 1.4μm pixel, leads to bottom and top diameters of 88nm and 152nm (Fig. 6). 800nm should be seen as a worst case, as the thickness of the PMD will lower in the next generations. Scaled 3D contacts are then compatible with 2D contact technologies.

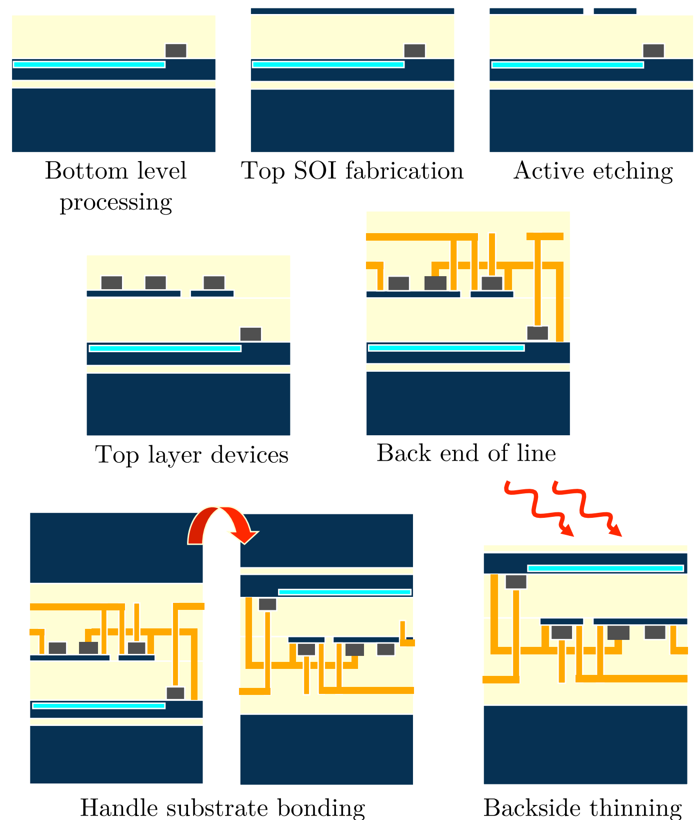

Fig. 5. 3D sequential integration process flow. Pinned photodiode/transfer gate are fabricated on an SOI substrate, followed by the realization of a silicon layer and subsequent low temperature transistor processing. Afterwards, 3D contacts and standard BEOL are realized. Finally, Backside illumination is achieved by bonding to a handle substrate and thinning the starting SOI substrate.

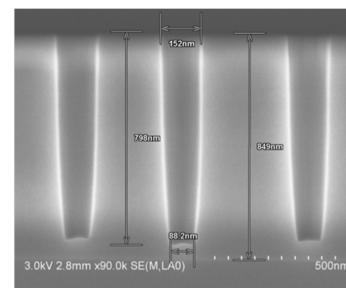

Fig. 6. High Aspect Ratio contact etching capabilities tested on 800nm SiO_2. Bottom and top critical dimensions (CD) are 88nm and 152nm respectively.

As a consequence of the sequential process, pinned photodiodes must endure top layer transistors fabrication. The admissible thermal budget has been set to 700°C 6h for 1.4μm pixels. At temperatures higher than 890°C

(Fig. 7), the diffusion of dopants induces an increase of the diode potential, with a shift of 540 mV (W/L 1.28/1.19μm) for 1113°C. V_{ch} is linked to the potential hump at the source side of the transfer Gate due to the P implant under the spacer. Diffusion of the P implants leads to a decrease of V_{ch}, which means that the potential hump increases and leads to potential lag. Finally, high performance logic transistors become unusable after 700°C 6h.

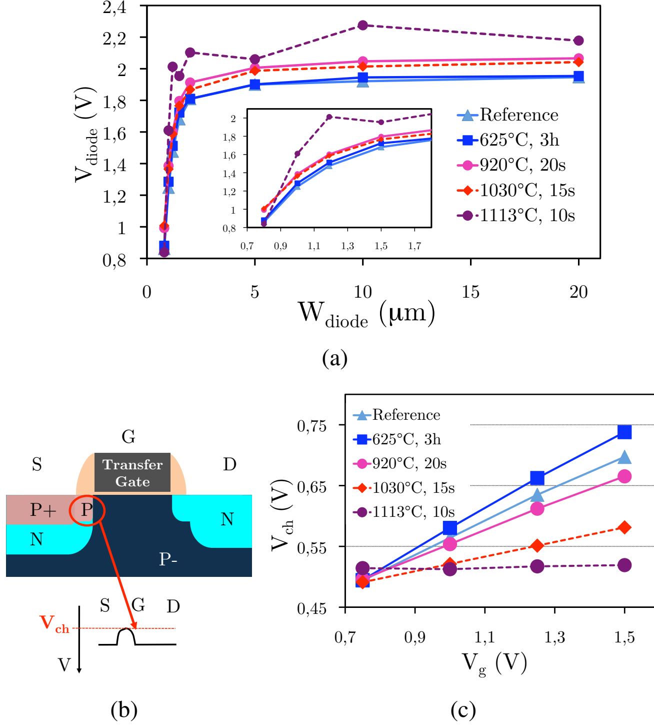

Fig. 7. Impact of annealing conditions on pixel specific devices. a) Diode potential (L=1.28μm). b) V_{ch}, defined as the height of the potential hump at the source of the Transfer Gate. c) $V_{ch}(V_g)$ for different: modulation is lost after Spike annealing at 1113°C.

After the photodiode fabrication on SOI substrates and the deposition of a 400nm PECVD oxyde layer (ILD), a 30nm Si film is transferred by room temperature direct bonding and etch-back of an SOI wafer. Subsequent annealing at 500°C led to a uniform bond across the wafer (Fig. 8), with energies of 1050mJ/m^2. Bonded SOI substrates have been thinned down to the BOX layer. Finally, the BOX has been etched with HF. A defect-free microstructure has been obtained (Fig. 8), with a surface roughness of 3Å rms in line with manufacturing specifications.

Pixel readout FDSOI transistors were then fabricated by a combination of low temperature processes including a HfO_2/TiN gate stack and a Solid Phase Epitaxy (SPE) for dopant activation at 600°C (Ge pre-amorphization at

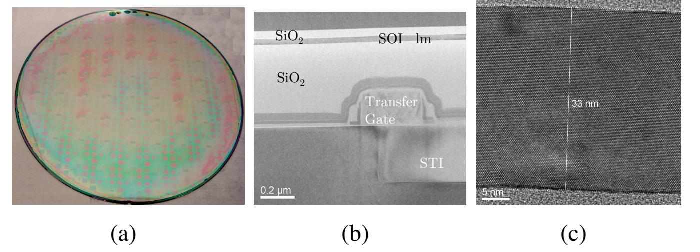

Fig. 8. a) Typical sample after thinning. b) TEM cross-section of the transferred SOI layer. c) Perfect crystallography is obtained and invisible bonding interface.

9 to 13keV, 5×10^{14} cm^{-2} [8] prior to S/D implantation). The benefits of the technique are illustrated in Fig. 9 [9] [10].

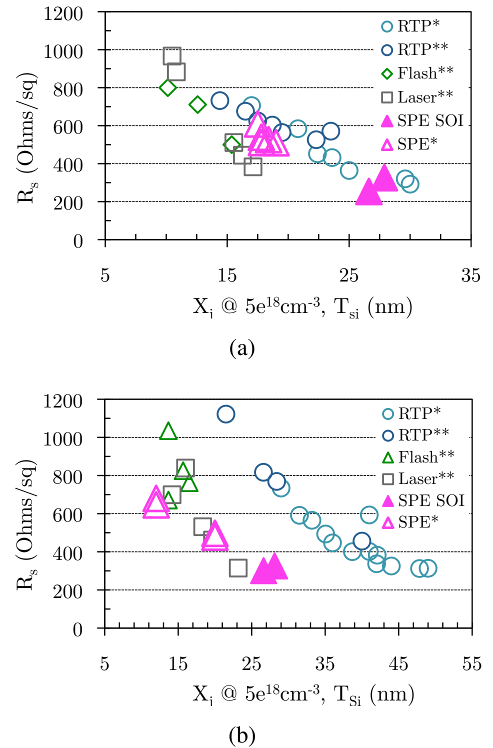

Fig. 9. a) Sheet resistance of N implanted silicon vs. X_j. b) Sheet resistance of P implanted silicon vs. X_j. * from [9], ** from [10], SPE SOI from [8].

IV. Performance perspectives

Special attention is paid on the low frequency noise [11]. The impacts of the high-k/metal gates and the low temperature process are studied: HfO_2/TiN devices are tested on 2D wafers. Normalized drain current *1/f* noise level plotted vs. I_d at 1 Hz shows a good correlation with $\Delta N - \Delta\mu$ model, even for the low temperature technologies (Fig. 10), the noise spectrum of HfO_2/TiN gates is dominated by three RTS sources (Fig. 11).

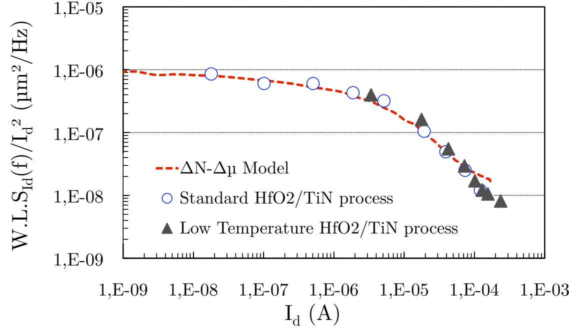

Fig. 10. Normalized drain current *1/f* noise level vs. I_d at a frequency of 1 Hz. A good correlation is obtained with the $\Delta N - \Delta\mu$ model.

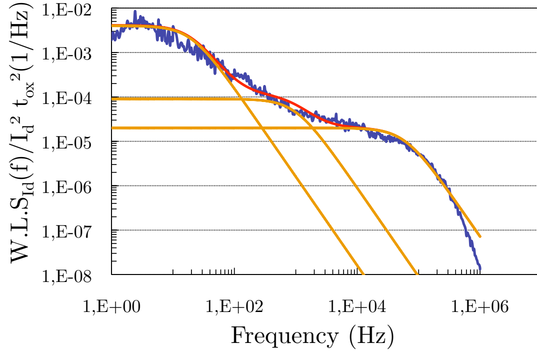

Fig. 11. Noise spectrum of a regular high temperature processed HfO_2/TiN gate transistor, dominated by three RTS noise sources.

HfO_2/TiN transistors are compared to conventional pixel technology in Fig. 12 where the PSD are normalized with t_{ox}. The HfO_2/TiN technology is two decades higher than the state-of-the-art technology, for high or low temperature processes. However, the gap decreases to a half-decade when compared to the 2.2μm pixel technology. Further improvements are found by increasing t_{ox} or designing a larger Source Follower (Fig. 13).

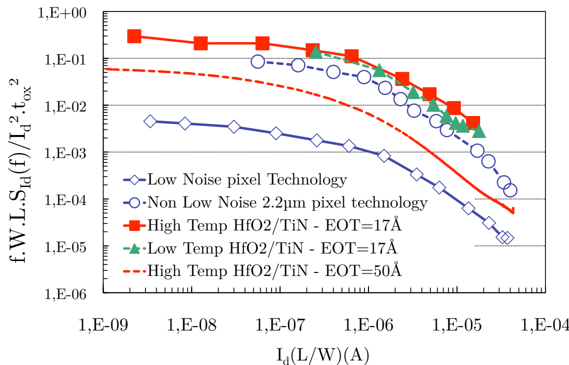

Fig. 12. PSD of High-k/Metal gate FDSOI transistors, including low temperature technology.

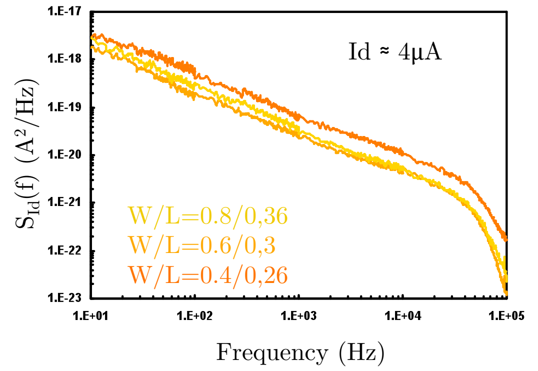

Fig. 13. Median value of the PSD for HfO_2/TiN gate transistors ($I_d \approx 4\mu A$): smaller transistors exhibit higher noise level.

V. Conclusion

The 3D integration of a miniaturized pixel faces dimensional challenges related to 3D contacts diameter and alignment precision. We have shown that an SOI-based 3D sequential integration is compatible with contacts diameters of 100nm. Combined with low temperature processing, it bypasses the weakness of the wafer-to-wafer alignment and tends towards the realization of low noise 3D miniaturized pixels.

References

[1] J. Prima *et al.*, "A 3 mega-pixel back-illuminated image sensor in 1t5 architecture with 1.45μm pixel pitch," in *International Image Sensor Workshop*, Jun. 2007, pp. 5–8.

[2] B. Pain, "Next generation cmos imaging - does soi hold the key ?" *IEEE International SOI Conference*, 2007, short Course.

[3] P. Coudrain *et al.*, "Setting up 3d sequential integration for back-illuminated cmos image sens with highly miniaturized pixels with low temperature fully depleted soi transistors," *International Electron Devices Meeting*, pp. 271–274, 2008.

[4] V. Suntharalingam *et al.*, "Megapixel cmos image sensor fabricated in three-dimensional integrated circuit technology," *Digest of Technical Papers, IEEE International Solid-State Circuits Conference*, pp. 356–357 Vol. 1, Feb. 2005.

[5] M. Koyanagi *et al.*, in *Proc. Digest of Technical Papers Solid-State Circuits Conference ISSCC. 2001 IEEE International*, 2001, pp. 270–271, 454.

[6] J. Burns *et al.*, "A wafer-scale 3-d circuit integration technology," vol. 53, no. 10, pp. 2507–2516, 2006.

[7] C. Chen *et al.*, "Scaling three-dimensional soi integrated-circuit technology," in *Proc. IEEE International SOI Conference*, 2007, pp. 87–88.

[8] P. Batude *et al.*, "Enabling 3d monolithic integration," *ECS Transactions*, vol. 16, no. 8, pp. 47–54, 2008.

[9] A. Pouydebasque *et al.*, "Cmos integration of solid phase epitaxy for sub-50nm devices," in *Proc. 35th European Solid-State Device Research Conference*, 2005, pp. 419–422.

[10] K. Suguro *et al.*, "Overview of the prospects of ultra-rapid thermal process for advanced cmosfets," in *Proc. International Workshop on Junction Technology*, 2004, pp. 18–21.

[11] C. Leyris *et al.*, "Impact of random telegraph signal in cmos image sensors for low-light levels," in *Proc. 32nd European Solid-State Circuits Conference*, 2006, pp. 376–379.