

A 1.4 μm Pixel Backside Illuminated CMOS Image Sensor with 300 mm Wafer Based on 65 nm Logic Technology

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Abstract

A 1.4 μm pixel size backside illuminated (BSI) CMOS image sensor has been successfully demonstrated. Fabrication process is based on a partial 65 nm logic technology with 300 mm wafer for the first time. Full color image has been obtained with VGA density test chip. Sufficient quantum efficiency (QE) curves with low crosstalk will be realized by isolation process modification.

Introduction

The main challenge in the pixel size reduction in CMOS image sensor is to overcome QE decrease because of narrow metal aperture and amount of optical stack over photo-diode (PD). Figure 1 shows optical stack height reduction trend with a pixel size. From 2.8 μm to 1.4 μm pixel pitch, stack height has actually been reduced by 1 μm per every pixel pitch generation to achieve required imager performance. According to this trend, 1.4-1.1 μm pixel stack height will become less than 1 μm . No room of wiring layer can be allowed on the PD because of the existence of color filter (CF) layers. BSI technologies [1-5] have already been reported as one of the solutions to overcome this problem. It is no need to have wiring layer over the PD in BSI structure.

On the other hand, not only a pixel performance but also advanced peripheral logic performance is required to meet the recent demand for a higher frame rate with a large image format. In addition to this, high productivity is also needed by imager markets. Therefore, 300 mm wafer product is strongly required. Figure 2 shows the examples of 300/200 mm wafer gross ratio according to chip size, which is one of the advantages of 300 mm technology. As shown in Fig. 2, actual gross ratio of 300/200 mm is more than calculated value which is area ratio of 2.25. From a technical point of view, process accuracy such as photo-lithography alignment used for backside fabrication steps with 300 mm equipment is higher than that of 200 mm, which would contribute to pixel optical performance improvement. The 300 mm

wafer manufacturing using advanced logic technology with high productivity is promising for 1.4 μm pixel CMOS imager and beyond.

Pixel Structure and Fabrication Technologies

Figure 3 shows pixel schematic used in this demonstration. The pixel adopts 1.4 μm pitch 2-way shared architecture. Fabrication process is shown in Fig. 4. The wafer used in this demonstration was 300 mm SOI wafer. The conventional front side illuminated (FSI) CMOS image sensor process based on a partial 65 nm logic technology was applied for MOS device fabrication. Fine patterned metal wiring was formed in the dielectric under a Si body. Thick insulator was deposited on top metallization and was well planarized by chemical mechanical polishing (CMP) technology. A handle Si wafer was bonded to the planarized top surface. Figure 5 shows IR image of 300 mm wafer after bonding. No voids and no defects were observed in entire surface. After backside substrate thinning, anti-reflection layer (ARL) was coated on the PD. Optical black metallization was formed on the backside surface. The CF and micro-lens (ML) were patterned on the ARL. Pad opening followed. Figure 6 shows SEM photograph of final pixel cross-section. The CF and ML are formed on the ARL over the PD.

Evaluation Results

The color images have been successfully obtained from the experimental VGA imager chip. The experimental VGA imager chip has an on-chip correlated double sampling (CDS) circuitry and an on-chip analog to digital converter (ADC). Figure 7 shows reproduced color image from the experimental VGA imager chip. Some rectangular patterns are observed in the color image shown in Fig. 7, but those patterns are not caused by an intrinsic noise but are caused by the test pixel block pattern laid-out in pixel array to obtain design data.

One of the key issues in BSI pixel design is a reduction of a color crosstalk. There are some key factors

in the design for crosstalk reduction. In this particular test pixel imager chip, electrical crosstalk is dominant factor for crosstalk. The PD used in this experimental chip is isolated by diffusion layer. In this experimental imager chip, isolation structure has not been fully optimized. In Fig. 8, B/G crosstalk averaged in 510 – 580 nm wavelength is compared between two different isolation structures, Isolation A and Isolation B. Isolation A is the isolation structure which the experimental imager pixel uses, and Isolation B is the optimal isolation structure based on the isolation technology already used in 1.4 μm FSI pixel. In Figure 8, crosstalk with Isolation A is a measured results and crosstalk with Isolation B is a simulated result. Reduction of the crosstalk is expected by using Isolation B technology. Figure 9 is simulated QE curves with Isolation B.

Dark current reduction is the other important issue in BSI pixel design. The strong dependence of dark characteristics on backside surface condition has been observed. Figure 10 shows dark images in two different backside conditions. Large and patterned higher dark current area was observed in the dark image from the imager chip with surface condition A, but no dark current pattern was observed in the dark image from the imager chip with surface condition B.

Summary

A 1.4 μm BSI pixel using 2-way shared architecture was fabricated with 300 mm wafer for the first time. The conventional FSI CMOS image sensor process based on a partial 65 nm logic technology was applied for MOS device fabrication. No voids and no defects were observed after wafer bonding.

Full color images have been successfully obtained from the experimental VGA imager chip. Reduction of the crosstalk is expected by using Isolation B technology which is the optimal isolation structure based on the isolation technology already used in a 1.4 μm FSI pixel. Sufficient QE curves with low crosstalk will be realized by isolation process modification.

Large and patterned higher dark current area was observed in the dark image from the imager chip with surface condition A, but no dark current pattern was observed in the dark image from the imager chip with surface condition B.

The 300 mm wafer manufacturing using advanced logic technology with high productivity is promising for 1.4 μm pixel CMOS imager and beyond.

References

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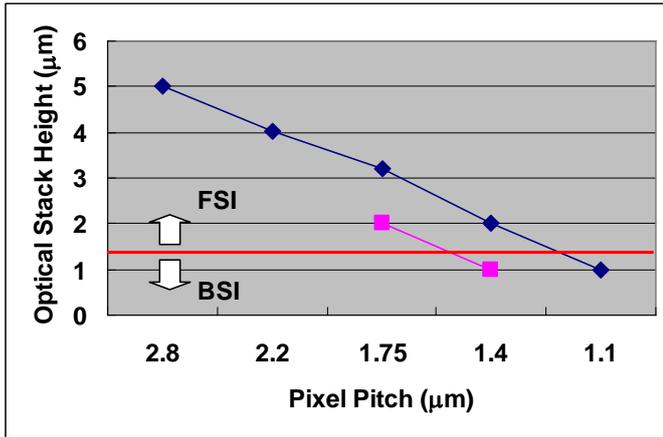


Figure 1 Optical stack height reduction

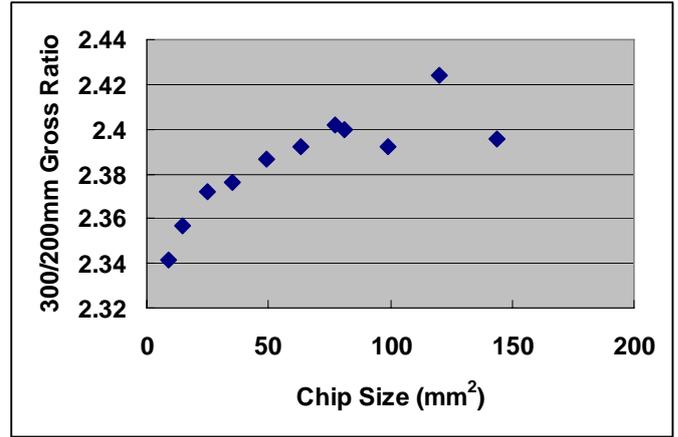


Figure 2 300/200 mm wafer gross ratio

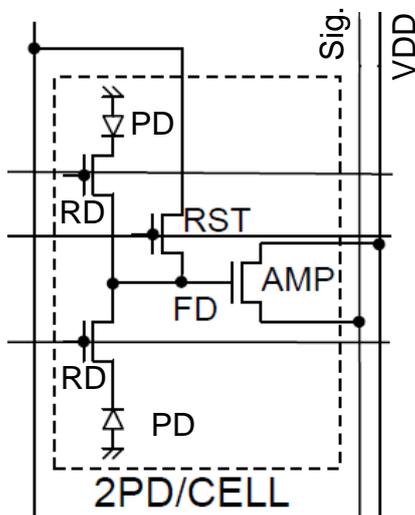


Figure 3 Pixel schematic with 1.4 μm pitch 2-way shared architecture

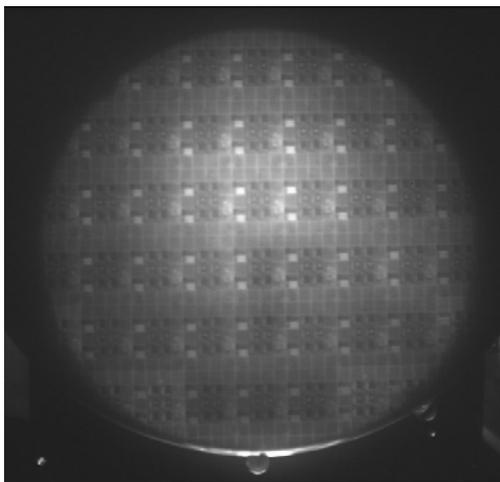


Figure 5 IR image of 300 mm wafer after wafer bonding

- 300 mm SOI wafer
- CMOS imager process
- Top surface planarization
- Handle wafer bonding
- Backside thinning
- Anti-reflection layer
- Metallization
- Color filter / Micro-lens
- Pad opening

Figure 4 Fabrication process

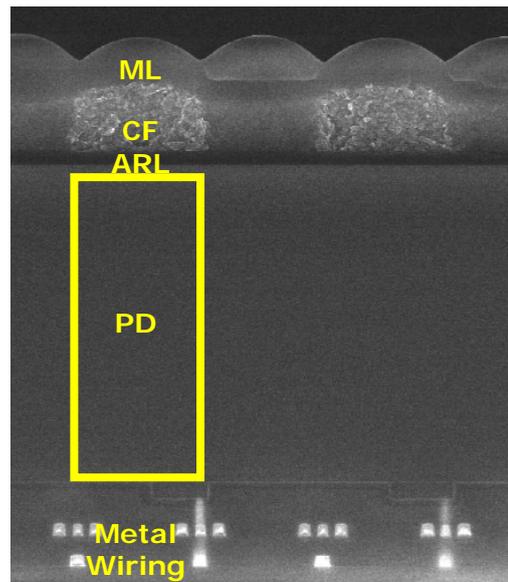


Figure 6 SEM photo of pixel cross-section



Figure 7 Reproduced color image from the experimental VGA imager chip

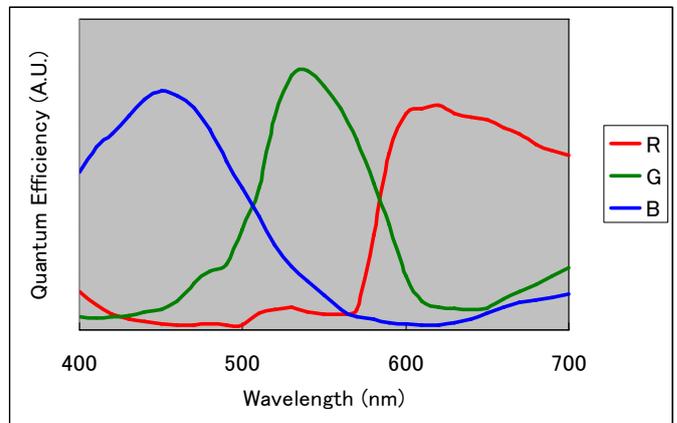
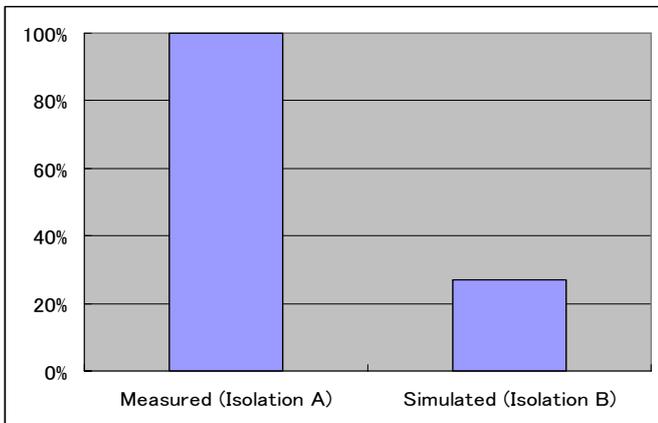
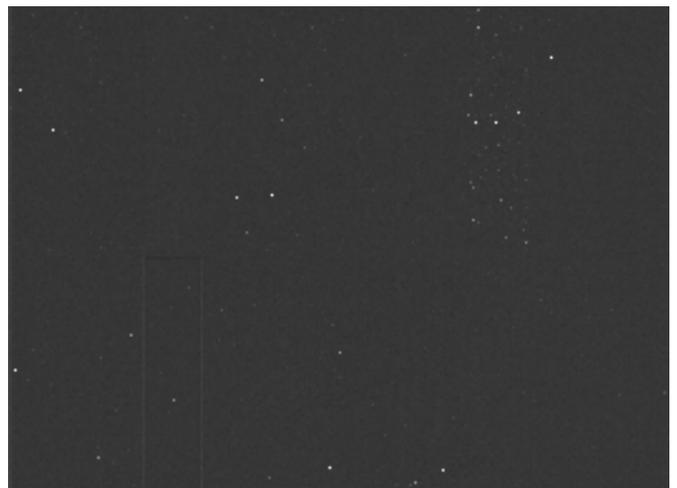


Figure 8 Comparison of average crosstalk of B/G (510nm-580nm) between the pixel with Isolation A (measured) and Isolation B (simulated)

Figure 9 Simulated QE curves with Isolation B



(a) Condition A



(b) Condition B

Figure 10 Dark images from the experimental imager chip