

A Manufacturable Back-Side Illumination Technology using Bulk-Si Substrate for Advanced CMOS Image Sensor

S.G. Wu¹, C.C. Wang, D.N. Yaung¹, Y.L. Tu¹, J.C. Liu¹, T.H. Hsu¹, F.J. Shiu¹, C.Y. Yu¹, G.Y. Shiau¹, R.J. Lin, C.S. Tsai¹, L. Tran¹, S.S. Chen¹, C.C. Wang¹, S.Y. Huang¹, H. Rhodes², D. Tai², Y. Qian², D. Mao², S. Manabe², A. Shah², R. Yang², J.C. Hsieh³, Calvin Chang³, C.W. Lu³, Shawn Tseng³

¹Taiwan Semiconductor Manufacturing Company, Hsin-Chu, Taiwan, R.O.C.

²OmniVision Technologies, Inc., 4275 Burton Drive, Santa Clara, CA 95054

³VisEra Technologies Company, Hsin-Chu, Taiwan, R.O.C.

Tel:(886)35636688 Ext.7082013, Fax:(886)35784848, E-mail: skwu@tsmc.com

Abstract

In this paper we report for the first time on the manufacturable technology of backside illumination (BSI) CMOS image sensor (CIS) on bulk CMOS wafer. To achieve low cost manufacturing, we simplify process flow and tighten manufacturing spec control to keep the level of particle, contamination and defect comparable with conventional FSI (front-side illumination) process. A reliable bonding process, together with wafer thin down process, were developed to increase the mechanical stability, minimize the crystal defect and maintain good thickness uniformity within the remaining Si. With the BSI process, device behaves the similar performance and reliability result as that with FSI process after detail characterization. Over 40% quantum efficiency (QE) and less than 1 e-/sec per pixel dark current at room temperature are achieved in 1.4um pixel by optimizing pixel and micro-lens (ML) design with 90nm node design rule. This technology has been in manufacture in a 200mm production line and being developed for a 300mm processing line for 1.1um pixel and beyond and demonstrates convincing manufacturing capability.

Introduction

CIS has been widely used due to many advantages as compared to CCD, such as low voltage, low power consumption, random access of the captured image data, compatibility with standard CMOS logic process technology, and realizing the integrated single-chip camera (1-4). As the sensor pixel size is continually scaled down to get higher resolution and multi-layer metal is adopted in conventional FSI, the pixel sensitivity degradation and crosstalk are getting worse because of optical scattering (Fig.1). Several approaches, such as thin backend and thin-film photodiode on ASIC, have been proposed to overcome the optical challenges. BSI is the most promising pixel structure with less impact on sensor chip function, especially for smaller pixel. Compared to FSI sensor, BSI sensor shows much better quantum efficiency and chief ray angle. However, BSI technology introduces more complicated processes. That lead to new challenges which FSI did not face, such as device reliability concern, remaining Si thickness uniformity control, backside Si surface damage, u-lens design, and so on. By adopting innovative design and process technology, we not only exhibit high performance 1.4um BSI sensor, but also successfully demonstrate BSI technology manufacturability.

Technology

P/P+ epi-wafer is chosen for a cost-effective BSI starting material instead of using SOI wafer. Fig.2 shows the process flow in backside technology. Thin-down process involves mechanical grinding and wet chemicals etch with optimal selectivity to stop on epi-Si. The remaining Si thickness control is shown in Fig.3a & b. for wafer-to-wafer uniformity and within wafer uniformity, respectively. By using a feed-forward system, wafer-to-wafer thickness variation within $\pm 0.025\mu\text{m}$ can be achieved. Within wafer uniformity can be improved to less than $\pm 0.1\mu\text{m}$ by using a well-controlled wet chemical recipe.

Laser anneal is used to activate backside P+ implant. Thermal simulation shows temperature of 600-800C at Si device area, although Si surface reaches melting temperature. Because of short pulse duration time, on the order of tenth to hundredth of ns, laser anneal has been demonstrated no impact to device from wafer acceptance test (WAT). After laser anneal, the remaining Si defect performance is characterized by TEM. During Si melting and re-crystallization, different levels of dislocation 020 & 022 are observed in the re-crystallized layer. By optimizing laser condition, crystal defect free can be achieved, as shown in Fig.4.

To reach manufacturing readiness, the goal is to minimize total defect dies. The major defect sources come from wafer thin-down process, weak wafer edge structure and film peeling. For Si thin down process, water mark generated

on hydrophobic Si surface during wet processes before thin down could act as a hardmask during wet chemical etch to form coin-like defects, as shown in Fig. 5. The major defects (surface particles and scratch) shown in Fig.6 were related to the weak wafer edge structure induced by lateral etch through bonding interface during wet chemical thin down. Progresses were achieved already to reduce defective dice to less than 10.

Device Design and Reliability

As long as final Si thickness is thicker than device well depth after BSI processing, MOS devices characteristics are in performance with those fabricated with FSI processing as shown in Fig.7. NMOS shows higher backside-illuminated Ioff than PMOS due to electron possess lower recombination rate. Thus, optical shield is needed for BSI chip to minimize device Ioff current and reduce standby current under illumination. Reliability check has passed GOI, hot carrier and EM tests. Fig.8 shows the impact of BSI charging effect on device Vt stability. After better charging control it can be improved significantly and pass Vt stability test as well.

For optical design associated BSI structure, ML owns larger curvature and better light collection rate due to shorter optical path and higher fill factor. As pixel size is continuously shrunk smaller than 1.4um, ML shape and gap become more critical. By using binary mask pattern design as shown in Fig.9, pixel sensitivity and color shading can be significantly improved at pixel corner and chip edge, respectively. It also helps to tighten ML gap then enhances SNR by improving QE and crosstalk as shown in Fig.10.

Pixel Optical Performance

BSI imager demonstrates superior quantum efficiency than FSI imager due to free of metal blocking layers and without multiple dielectric stack films to reflect light in the optical path. Fig.11 shows QE plots of 1.75um FSI vs. BSI pixels for wavelength between 300nm to 700nm. 40% to 60% higher QE in R/G/B color band is observed with a 1.75um pixel-size 2M-pixel test chip, which is implemented by a 90nm node 1P3M BSI technology. 60% blue and green peak QE can be achieved, which is much better than existing CMOS image sensors with FSI technologies.

Crosstalk is another important parameter which influences color performance. BSI imager shows ~30% to 80% lower crosstalk values than FSI imager at all color bands. The mechanism can be explained as follows. For FSI imager, a deep P-well implant is typically implemented as an isolation barrier to prevent the photo-generated electrons to diffuse across to the adjacent pixel. However, the implanted deep P-well dopants are difficult to reach the bottom of the epi layers due to the limitation of maximum photo resist thickness and required resolution. If a thinner epi wafer is adopted to create the isolation barrier from top to bottom of the epi wafer, QE would be degraded too much to an unacceptable level, especially for red light. Therefore, the epi thickness becomes a tradeoff factor between QE and crosstalk in FSI imagers. For BSI imagers, due to better QE performance described above, the final Si thickness can be thinner to implement a top-to-bottom isolation barrier. As a result, the crosstalk of BSI imager is better than FSI imager.

Deviation of the final epi thickness shows the influence on QE. Fig.12 shows that an optimized final epi thickness achieves maximum QE for the R/G/B color bands. As Si thickness is 0.3um thicker, the blue QE is degraded due to carrier recombination by longer path for carriers to diffuse to photodiode. If the Si thickness is 0.3um thinner, the red QE is reduced by 3% due to less absorption in Si. Therefore, the final epi thickness control within wafer, within lot, and lot-to-lot variation plays a critical role in BSI imager process.

Conclusion

A manufacturable backside illumination technology for CMOS sensor has been reported in this paper. The starting material is bulk wafer instead of SOI wafer. Special modules are developed to tightly control remaining Si thickness, minimize contamination and particles. The 90nm CMOS BSI technology is implemented on a 1.4um 8Mega-pixel imager with superior angular response and low cross talk. The R/G/B QE can reach larger than 40% and the dark current is < 1 e-/sec at room temperature. This technology platform has been in manufacture in a 90nm node production line and being developed for 65nm node baseline for 1.1um pixel and beyond.

Reference

- [1]R. M. Guidash, IEDM Tech. Dig., pp.927-929, 1997.
- [2]Sunetra K. Mendis, IEDM Tech. Dig., pp.583-586, 1993.
- [3]Hon-Sun Wong, IEDM ED, pp.2131-2142, 1996.
- [4]Hi-Deok Lee, IEEE ED, pp.1848-1850, 1998.

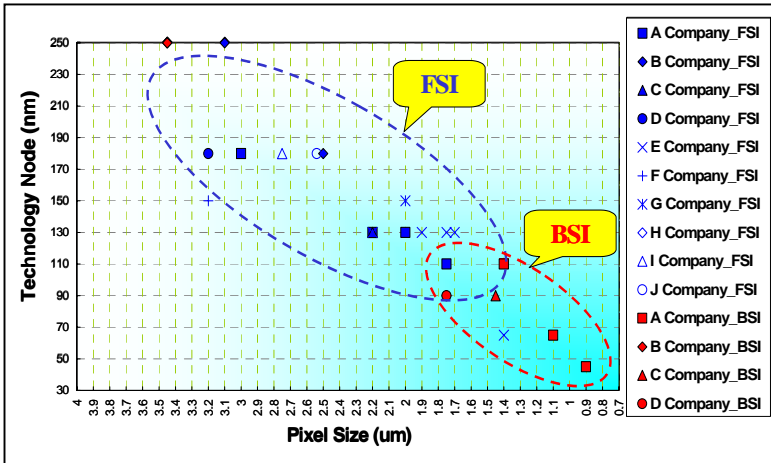


Fig.1: Scaling trend of CIS pixel size.

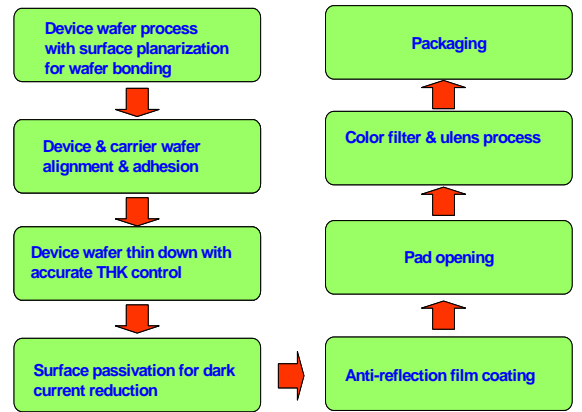


Fig.2: Schematic of BSI process flow.

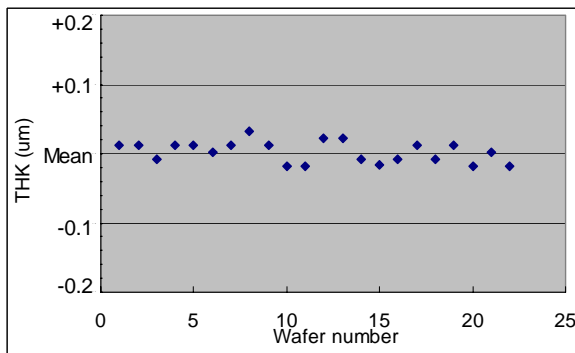


Fig.3a: Wafer-to-wafer thickness variation for epi-wafer thin down.

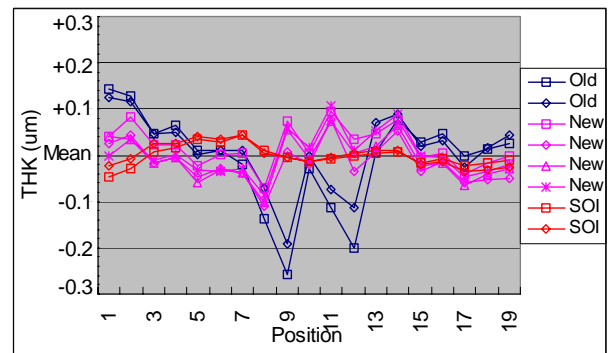
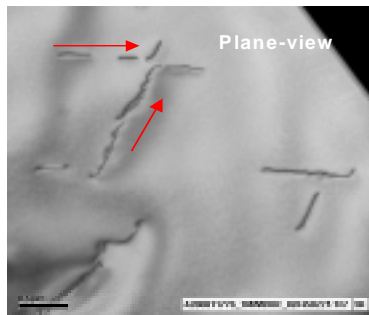
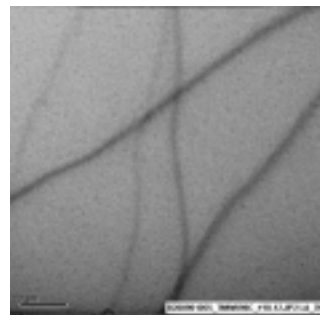


Fig.3b: Si thickness control by SOI vs Epi.



Defect density ~0.567/um



Defect free

Fig.4: Plane-view TEM shows (020) & (022) dislocation and defect free after laser anneal.

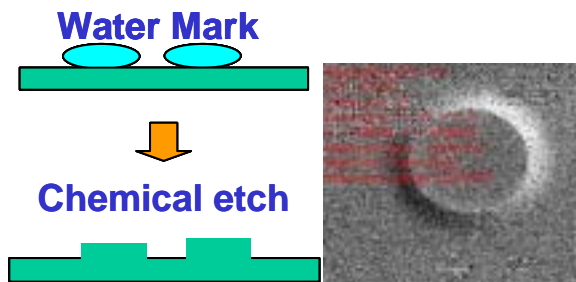


Fig.5: Wet thin down induced coin defect

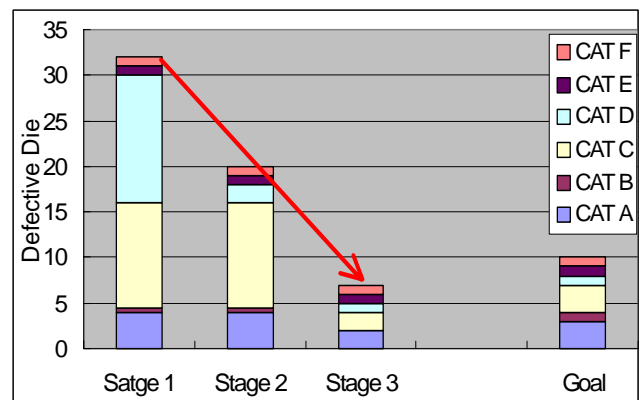


Fig.6 Defect monitor with KLA inspection.

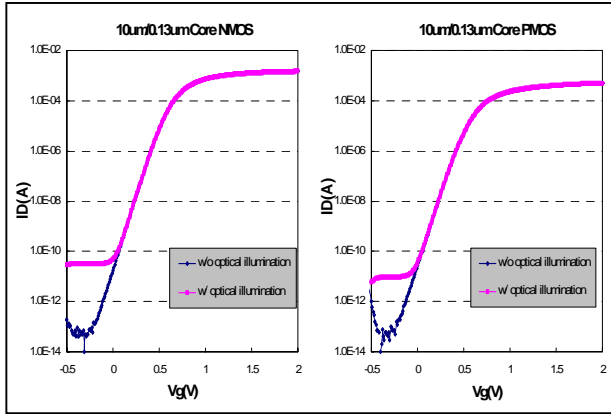


Fig.7: N/PMOS I-V curves under backside illumination.

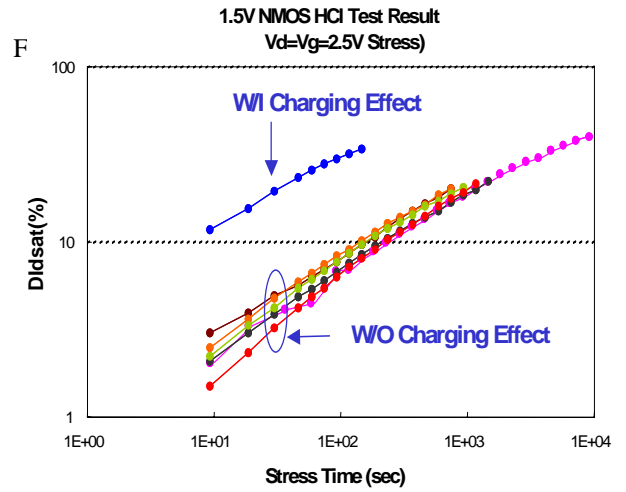


Fig.8: Vt stability degradation caused by charging effect.

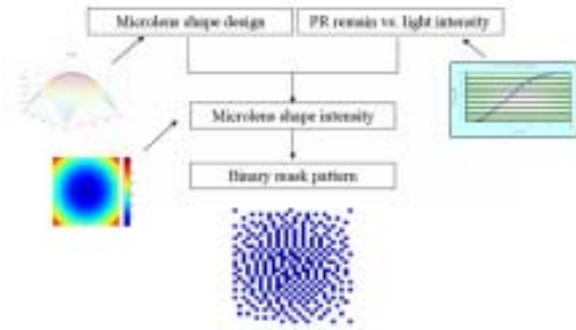


Fig.9 Binary mask pattern to improve u-lens shape

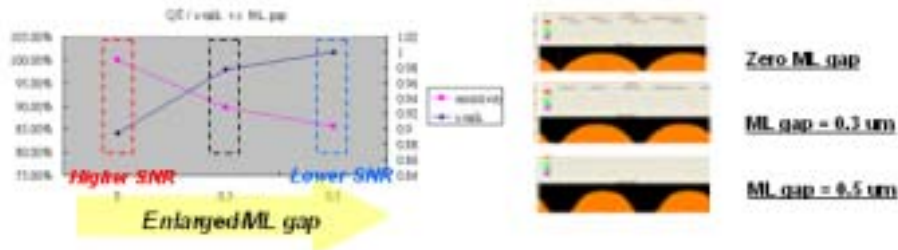
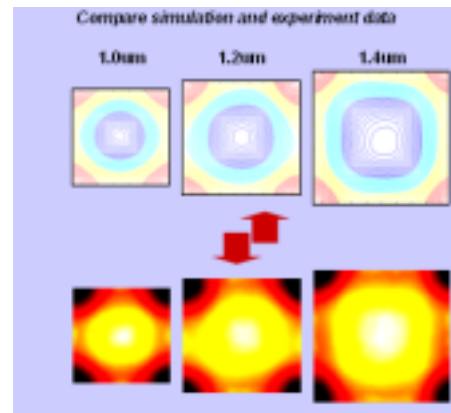


Fig.10 The impact of U-lens gap on QE and crosstalk.



Fig.11: QE for 1.75um FSI vs BSI.

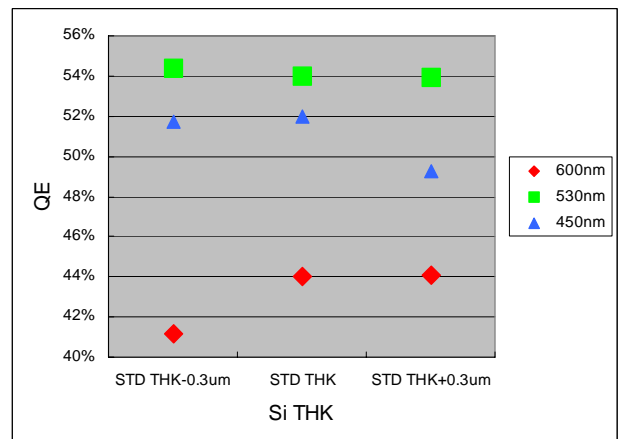


Fig.12: 1.4um pixel QE vs Si