

## Improved colour separation for a backside illuminated image sensor with 1.4 $\mu\text{m}$ pixel pitch

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### **Abstract:**

We demonstrate a back illuminated colour image sensor with a 1.4 $\mu\text{m}$  pixel pitch. A novel backside adapted pinned deep diode on n-substrates has been developed and characterized in order to achieve an improved colour separation. High quantum efficiency around 60% in the visible light spectrum has been attained whereas the other parameters stay in line with standard front side illuminated image sensors.

### **Introduction:**

Backside illuminated (BSI) CMOS image sensors have been reported as a possible solution for the 1.4 $\mu\text{m}$  pixel pitch and below [1]. Beside the multiple advantages, like 100% fill factor, lower optical stack and higher metal packaging density [2-4], the BSI sensors also point out several design and process challenges, like the backside to frontside alignment and the electrical crosstalk [3-4]. We have realized a colored BSI CMOS image sensor demonstrator with a 1.4 $\mu\text{m}$  pixel pitch in 1T5 architecture and a deep pinned photodiode on n-substrates for effective interpixel junction isolation, resulting in crosstalk improvement. The quantum efficiency (QE) has been improved by a factor of 2 in comparison to a simple frontside conventional diode, which is illuminated from the backside. The other parameters are in line with standard front side illuminated image sensors.

### **Pixel Design:**

The front-end design of the backside illuminated image sensor is based on a 0.13 $\mu\text{m}$  CMOS process. The backend metallization has been realized in 90nm copper based design rules. The pixel architecture consists of a pinned photodiode with transfer gate for reset noise cancellation due to correlated double sampling (CDS). Each pixel has a diode and a transfer gate transistor (TG). In order to increase the fill factor, four pixels are regrouped to one sensing node, which is connected to a RESET transistor and to a source follower (SF) transistor. With the READ transistor placed in the column circuitry, the average number of transistors per pixel is 1.5 (1T5 architecture, see figure 1).

### **Process & Experiments:**

The process flow is summarized in figure 2: After the CMOS imager frontend and backend realisation on SOI substrates a waferbonding layer (WBL) is

deposited and prepared for wafer bonding on a support wafer. Once the wafers are bonded and backside thinned, an anti-reflective coating is deposited, the pads are reopened from the backside and subsequently colour filters (CFA) and microlenses are processed. The alignment of the backside CFA and microlenses to front side layers was controlled by standard production FRAME-in-FRAME overlay controls (figure 3) and mappings (figure 4). The circuit transfer process (bonding and thinning) has been improved in order to decrease the layer deformation after transfer. A layer deformation, which is compatible with the colorization alignment specs, has been achieved thanks to these improvements (figure 4).

Three process approaches have been tested in order to improve electrical crosstalk, which is inherent to backside illuminated image sensors: thin p-epi layers, graded p-epi layers and a novel backside adapted pinned deep diode, realized on n-substrates.

If the photo sensitive layer (epi-layer) gets thinner, the photo generated electrons have to cover a shorter distance in order to reach the diode. Thus they have a lower possibility to diffuse into the neighbouring pixels. Figure 5 shows the comparison between a 1.0 and 1.5 $\mu\text{m}$  epitaxial layer. We observe a decrease of crosstalk for thinner substrates for the benefit of higher quantum efficiency. Nonetheless this approach of frontside conventional photodiode still induces too much QE losses.

Likewise in combination with frontside conventional photodiodes, doping gradients have been realized by adding boron during the epitaxial growth process. The boron doping gradient (see figure 6), creates an electric built-in field, which pushes the photogenerated electrons to the photodiode. The introduction of the graded p-doping profile results in a limited crosstalk improvement. The modulation transfer function (MTF) at Nyquist/4 has been improved by at least a factor of 2 in the visible spectrum.

A novel backside adapted pinned deep diode architecture on n-substrates has been simulated (figure 7) and processed. This deep diode can be subdivided into two parts: A first collecting and storing diode on the illuminated side, with a natural built-in electrical field. This first diode guarantees the collection of photogenerated electrons to the storage diode (figure 8). The storage diode is located at the

opposite of the illuminated side. The interpixel isolation has been realized by p-implants at multiple energies and doses, in order to create a junction isolation wall. These isolation walls are 4-11 times more effective by replacing the standard p-substrate by an n-substrate (figure 9).

***Pixel performances of the pinned deep diode on n-substrates:***

The conversion gain of the image sensor is  $70\mu\text{V}/e^-$ . We notice a significant improvement of the QE by the introduction of the deep diode on n-substrates. The QE increases to 60% in the blue spectrum and to 50% in the green spectrum, attended by a corresponding decrease of crosstalk, as can be seen in (figure 10). We attribute these enhanced performances to the effective interpixel isolation and to a very good drift of the photogenerated electrons to the diode. The red signal can be improved by 10% QE by means of a broadband antireflective filter (figure 11). Figure 11 also shows the extrapolation of QE gain in case of a thicker epitaxial layer at  $4\mu\text{m}$  instead of  $2\mu\text{m}$ . It was assumed that the crosstalk increases in the same relation as the absorption. This simulation shows that the QE can be higher than 65% for the blue, green and red spectrum due to an improved antireflective coating layer and a higher absorption in thicker epitaxial layers. The full well diode saturation charge is as good as for standard frontside diode. The dark current is  $1e^-/s$  at  $25^\circ\text{C}$ . The low dark current has been achieved thanks to dedicated frontside and backside process steps such as  $p^+$  pinning layer and thermal treatment. Thanks to a very good charge transfer, the lag is below the measurement threshold. Figure 12 shows a colour picture, taken with the discussed image sensor demonstrator with deep diode on n-substrate at 500lux, 15 frames per second, f-number 2.8. The

main image sensor parameters are summarized in table 1.

***Conclusion:***

We have demonstrated a back illuminated colour image sensor with a  $1.4\mu\text{m}$  pixel pitch. Due to the introduction of a deep diode in n-substrates, resulting in an effective interpixel isolation and an enhanced drift of photogenerated electrons to the diode, we obtained a significant improvement of QE with 60% in the blue spectrum and 50% in the green spectrum. The application of a broadband antireflective filter and thicker epi substrates will lead to a QE higher than 65% in the blue, green and red spectrum.

***Acknowledgements:***

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**References:**

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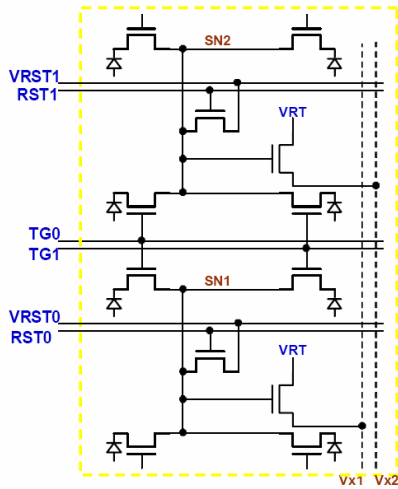


Figure 1: 1T5 pixel schematic

- SOI wafer
- CMOS Imager Process
  - FE 130nm
  - BE 90nm Cu
- Wafer Bonding Layer (WBL) Deposition and Preparation
- Wafer bonding and backside grinding
- Anti-reflective-coating (ARC)
- Pad opening
- Color Filters and Micro-Lens processing

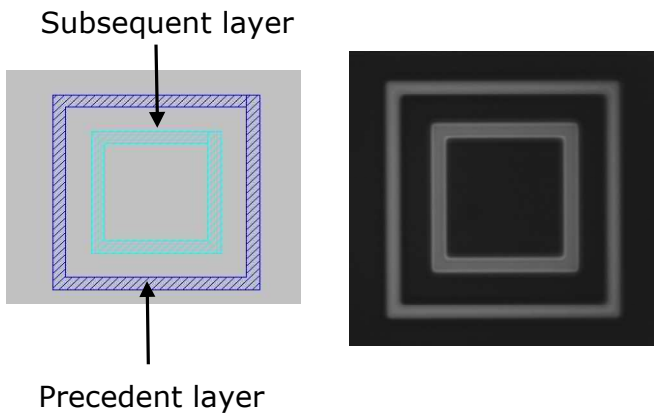


Figure 3: Left: Principle of FRAME-in-FRAME overlay control; Right: Overlay control of backside layer to frontside layer

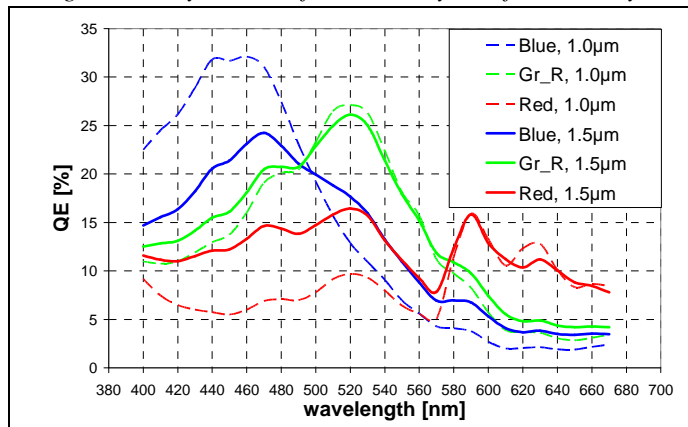


Figure 5: Comparison of QE of 1.0 and 1.5µm thick epitaxial SOI substrates (conventional diode)

Figure 2: Process flow

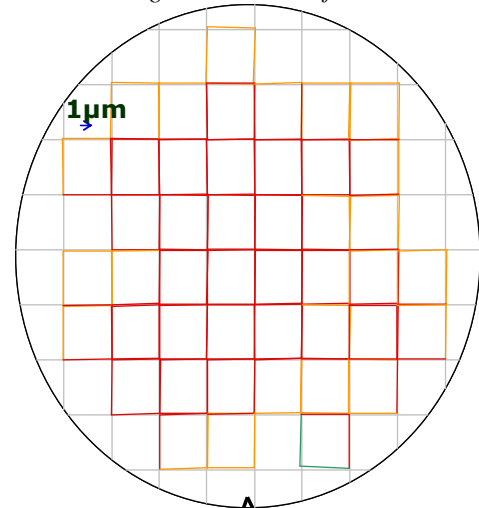


Figure 4: Mapping of overlay control, showing a layer deformation of the bonded wafer, which is compatible to colorization alignment

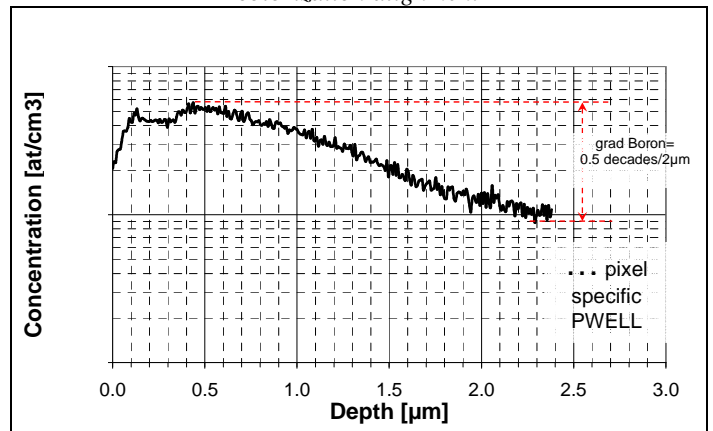


Figure 6: SIMS of sample with a boron gradient of 0.5 decades. The corresponding electrical drift field is 20 mV/µm

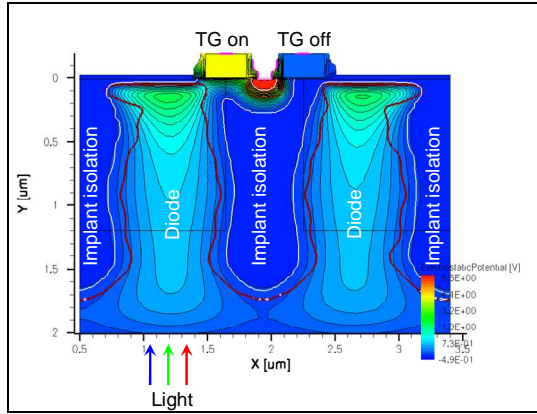


Figure 7: Simulation of deep diode on n-substrate

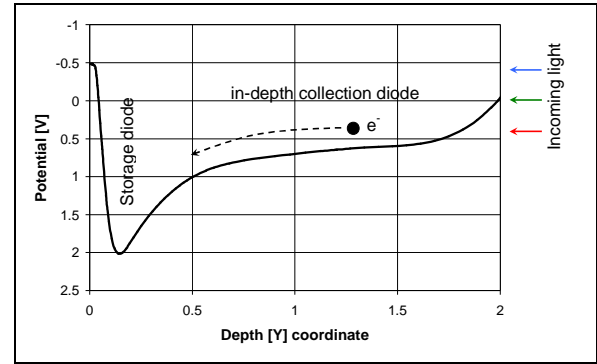


Figure 8: Potential profile of deep diode on n-substrate

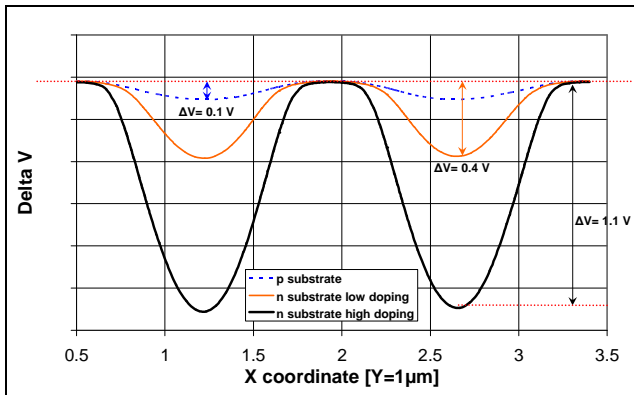


Figure 9: Comparison of potential walls in p- and n-substrates

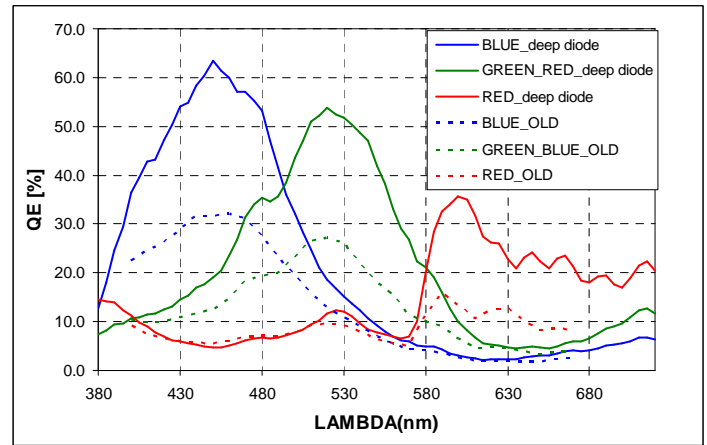


Figure 10: Comparison of QE for BSI imager with new deep BSI diode and conventional FSI diode

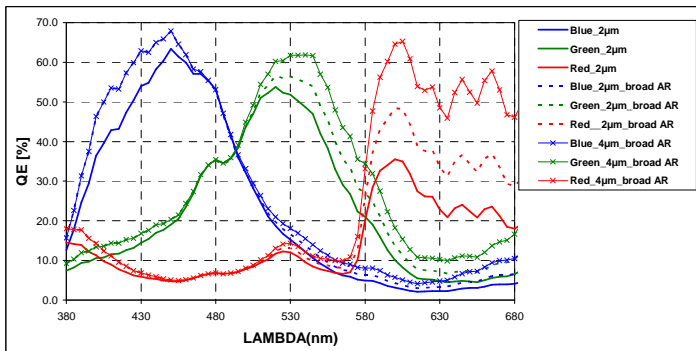


Figure 11: Comparison of QE of deep diode with 2µm epi, 2µm epi with improved broadband AR. Extrapolation of 4µm epi with broadband AR



Figure 12: Image, taken with back-illuminated image sensor demonstrator in 1T5 architecture with 1.4µm pixel pitch, deep diode on n-substrate

	1.4µm back illuminated pixel	Comment
Conversion Gain [ $\mu\text{V}/e^-$ ]	70	
Lag [ $e^-$ ]	0	Charge transfer free of lag
Dark Current at 25°C [ $e^-/s$ ]	1	Mean Value
Temporal Noise [ $e^-$ ]	5	Main contributor: SF

Table 1: Performances of colored back-illuminated image sensor demonstrator in 1T5 architecture with 1.4µm pixel pitch, deep diode on n-substrate and interpixel isolation by implant