# High Performance CMOS Image Sensor for Low Light Imaging

**Xinqiao (Chiao) Liu, Boyd Fowler, Hung Do, Steve Mims, Dan Laxson, and Brett Frymire**
Fairchild Imaging, Inc., 1801 McCarthy Boulevard, Milpitas, CA 95035

## Abstract

We present a prototype CMOS image sensor (CIS) intended for low light imaging applications. The prototype sensor contains 320 x 240 pixels with 36 different pixel architectures. Pixel size is 10.8 μm x 10.8 μm. The measured QE is 55% at 555nm, dark current is 11pA/cm$^2$ at 30 ˚C, read noise is 1.9e- RMS operating at 30 Mpixels/sec, and the conversion gain is 1046 μV/e-. We present the pixel design that achieved the best performance taking into account dark current, image lag, QE, and read noise. We also describe the low noise readout circuitry that achieves the lowest read noise published to date for any area CIS.

Keywords: CMOS, image sensor, CIS, scientific image sensor, FPA, low light level, read noise

## Introduction

Many scientific, medical and industrial imaging applications demand low-light solid-state focal plane sensors that have photon counting sensitivity, megapixel or higher resolution, and hundreds or even thousands of frames per second readout speed. Some examples include live-cell fluorescence microscopy, DNA sequencing, electron microscopy, X-ray crystallography, and security surveillance. To achieve high sensitivity, the sensor needs to have very low dark current (ideally less than 1e-/pixel/frame at 60 ˚C), very low read noise (ideally less than 1e-), and very low image lag (ideally less than 1e- per transfer since image lag introduces excess noise). Further, the sensor needs to high QE (>50%), high MTF (>50% at Nyquist), good linearity, and good uniformity (PRNU <2%).

The introduction of the pinned photodiode technology and the advance of low noise readout circuitry have dramatically improved the image quality of CMOS image sensors [1], [2]. These developments are rapidly making CMOS sensors the preferred technology for developing new high-performance low-light image sensors.

Fairchild Imaging has always been at the forefront of the high performance imaging development. Previously we presented a CCD / CMOS hybrid focal plane array for low light level imaging applications [3]. In this paper, we present a prototype monolithic CMOS image sensor design that further enhances our low light imaging capabilities. The sensor has a measured conversion gain of 1046 μV/e-, a dark current density of 11pA/cm$^2$ at 30C, and sensor read noise of 1.9e- RMS operating at 30 Mpixels/sec.

In the following sections, we present the pixel design that achieved the best performance taking into account dark current, image lag, QE, and read noise. We will also describe the low noise readout circuitry that achieves the lowest read noise published to date for any area CIS.

## Sensor Architecture

The prototype sensor was fabricated using a 0.18 μm CMOS image sensor process through a commercial foundry. The process features a pinned photodiode for low dark current and specially engineered pixel transistors for improved voltage swing and low 1/f noise. The design also features a thinned backend process with reduced the stack height. Figure 1 shows the chip layout and Figure 2 shows the block diagram. The prototype sensor contains 320 x 240 pixels with a total of 36 different pixel designs. The sensor has two analog output ports and can operate at up to 30 Mpixels/sec per output port. The pixel size of the sensor is 10.8 μm x 10.8 μm. Figure 3 shows the analog signal chain schematic. The signal path includes the pixel circuit, column amplifier, sample and hold capacitors, and analog multiplexing circuit.

Contact info: chiao.liu@fcimg.com, (408) 433-2605

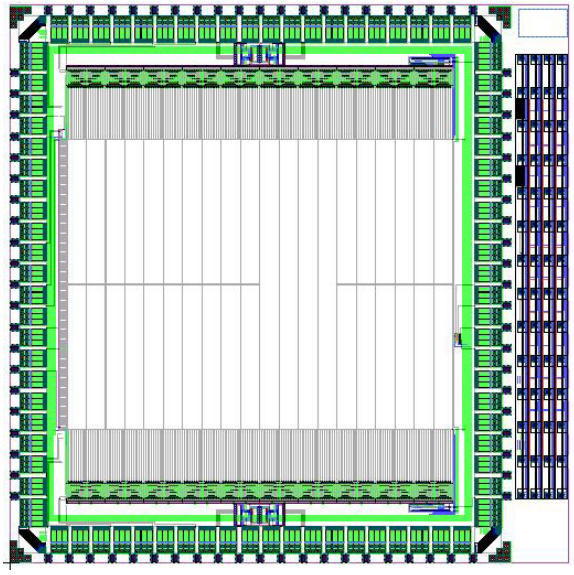

**Figure 1**. Prototype chip layout

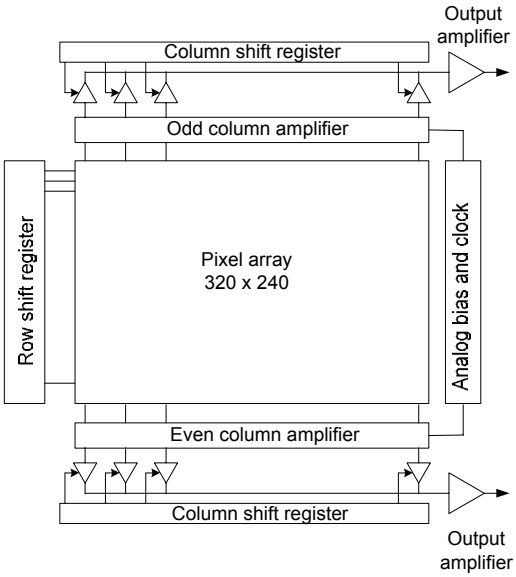


**Figure 2**. Sensor block diagram

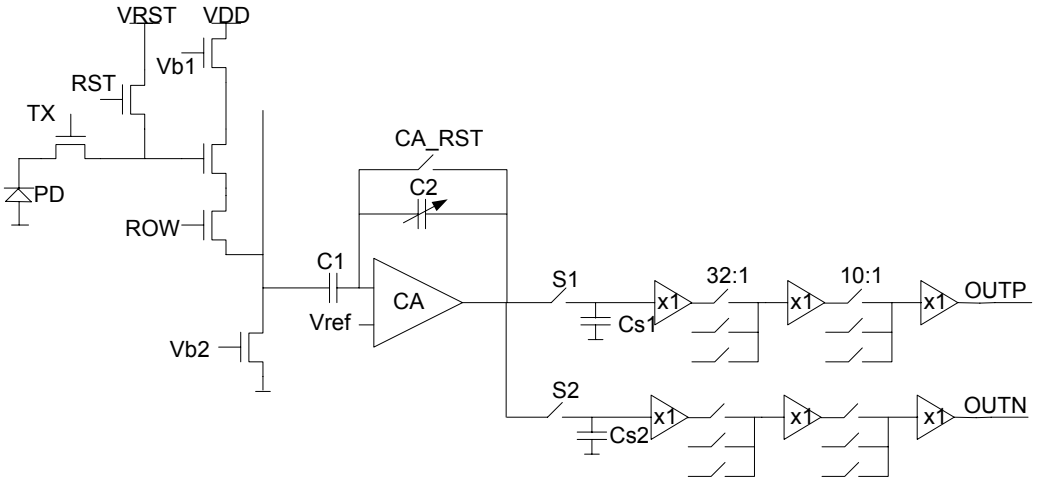


**Figure 3**. Analog readout signal chain

The 10.8 µm pixel employs a 5T APS circuit where the fifth transistor on top of the source follower transistor is used for power supply noise rejection and impact ionization noise reduction. The column amplifier has two gain modes: a high gain mode of 1046 µV/e- and a low gain mode of 32 µV/e-. The full well capacity is limited by the final output voltage swing in high gain mode with a well capacity of 1.4 ke-; and it is limited by the voltage swing at the floating diffusion node in low gain mode with a well capacity of 30 ke-. The column amplifier bandwidth was carefully adjusted such that minimum thermal noise contribution from the amplifier is achieved in high gain mode. To reduce the 1/f noise, the size of the source follower transistor inside the pixel is larger than minimum size.

Pixel reset noise is cancelled by the correlated double sampling circuit. The two sampling capacitors at the column amplifier output further reduce the KTC noise due to the column amplifier reset transistor. The sampled reset and signal voltages are multiplexed and read out in pseudo differential mode such that the common mode noise coupled from other sources can be further eliminated at the off-chip differential ADC.

## Pixel Design Optimization

A total of 36 different pixel designs are in the main array. Pixel variations are intended to help optimize critical sensor parameters such as dark current, QE, image lag, and read noise. Figure 4 shows the cross section of the pinned photodiode. The varying parameters within different designs include the distance from the buried diode to the STI edge (d1), the overlap of the transfer gate threshold adjustment implant, and the size and shape of the photodiode (d2).

Figure 5 shows a typical pixel layout, where the green region is the photodiode and the grey region is the active area. The effective pixel fill factor is 81%. Color filters and micro-lenses were not used in the fabrication of this chip. The large pixel area of this design provides a lot of freedom to optimize pixel architecture in order to achieve superior low-light imaging performance. Such opportunity is not available in small pixel designs where the architecture is strongly constrained by the limited pixel area.

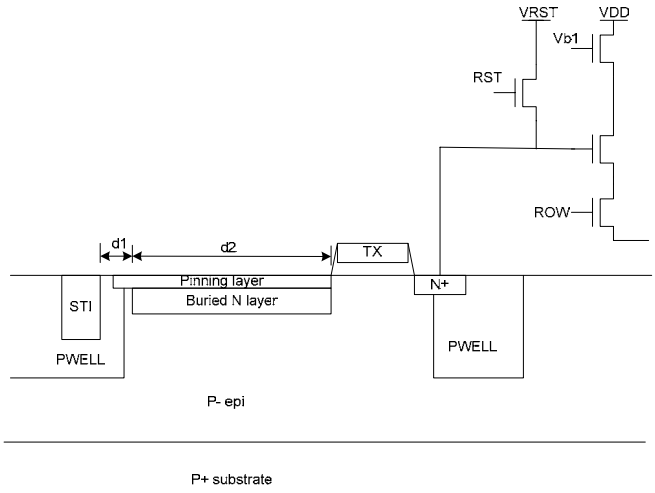


Figure 4. Pixel cross section

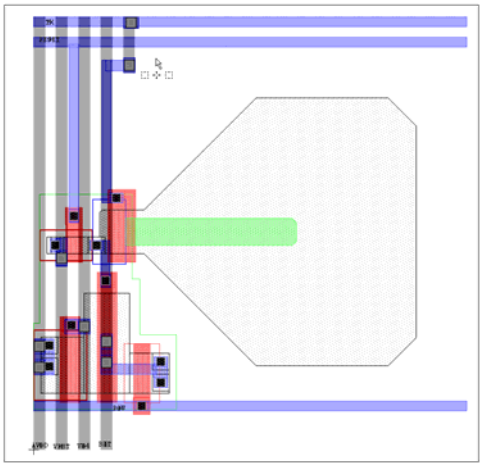

Figure 5. Typical pixel layout

## Measurement Results

Figure 6 is a measured photon transfer curve. A conversion gain of 1046 μV/e- was achieved by reducing the floating node capacitance and using a high-gain column amplifier. The non-linearity of the sensor is less than 0.5%. Figure 7 shows the dark current density histogram of one pixel design. The mean dark current density of 10.8 pA/cm$^2$ was achieved by separating the photodiode edge from STI edge by 1 μm. The histogram also shows white pixels at higher dark current levels. Figure 8 shows the sensor read noise histogram with a mean value of 1.9e- and standard deviation of 1.2e-. The noise measurement was performed at 30 Mpixel/sec output rate, since the readout circuit was designed for a 1k x 1k sensor operating at 30 frames/sec. Further investigation of the noise source revealed that a majority of the noise is a result of the charge transfer operation. The read noise was reduced to 0.7e- RMS if TX gate was maintained low. Detailed modeling and analysis of the charge transfer noise are presented by another paper in this conference [4]. Table 1 summarizes the measurement results of the various pixel designs.

## Summary

In this paper, we presented a prototype CMOS image sensor designed for low-light imaging applications. The initial results are encouraging, especially the low sensor readout noise, low dark current, and high sensitivity. These combined with the inherent low power and high speed potential of CMOS imager sensors will enable this technology to make further inroads into high performance imaging applications previously dominated by CCDs.

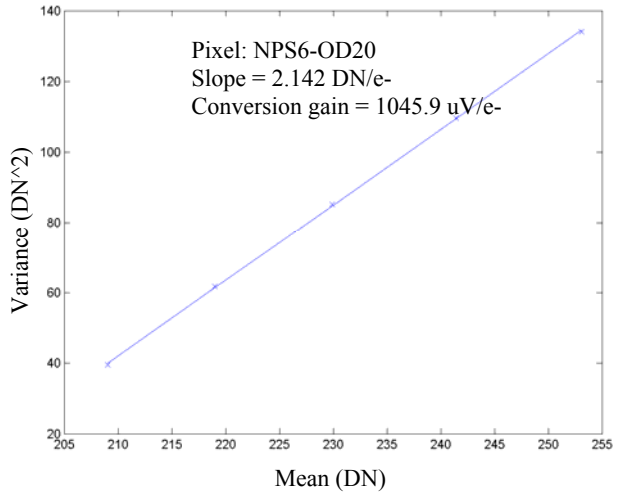


**Figure 6.** Photon transfer curve and the conversion gain

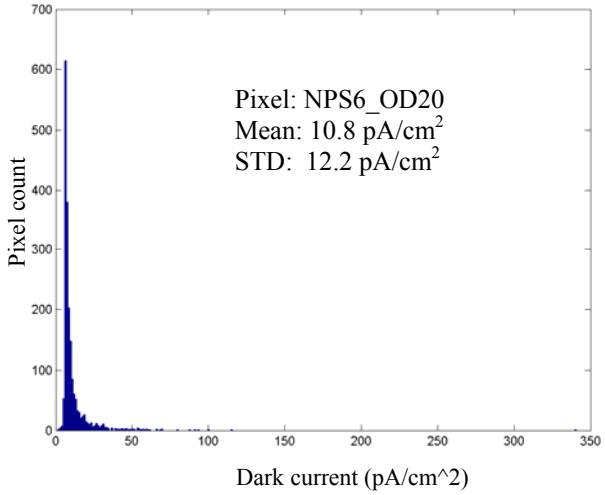


**Figure 7.** Dark current distribution

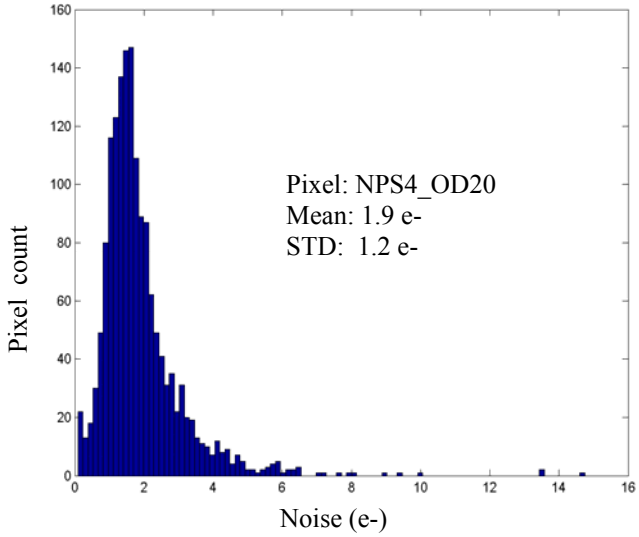


**Figure 8.** Read noise distribution

| Pixel | Conv gain (uV/e-) | Dark current (pA/cm^2) | Read noise (e-) | QE (550nm) | Lag |
|---|---|---|---|---|---|
| NPS2_OD10 | 999 | 9.0 | 2.5 | 48.5% | 0.24% |
| NPS4_OD10 | 1034 | 10.1 | 2.4 | 52.4% | 0.17% |
| NPS6_OD10 | 1088 | 10.3 | 2.4 | 50.8% | 0.15% |
| NPS6_OD20** | 1046 | 10.8 | 2.5 | 53% | 0.18% |
| NPS4Q_OD10 | 1189 | 10.5 | 1.9 | 44.9% | 8.72% |
| NPS7Q_OD10 | 1254 | 10.8 | 2.5 | 49.3% | 38.4% |

**Table 1**. Measured results of various pixels


## Acknowledgement

The authors would like to thank David Wen, Paul Vu, and Steve Onishi for technical discussions and supports.


## References:


[1] Y. Nitta, et. al., "High-Speed Digital Double Sampling with Analog CDS on Column Parallel ADC Architecture for Low-Noise Active Pixel Sensor", IEEE International Solid State Circuit Conference, Dig. of Technical Papers, 2006

[2] A. Krymski, N. Khaliullin, and H. Rhodes, "A 2e- Noise 1.3Megapixel CMOS sensor", 2003 IEEE Workshop on Charge-Coupled Devices and Advanced Image Sensors

[3] X. Liu, B. Fowler, S. Onishi, P. Vu, D. D. Wen, H. Do, and S. Horn, "CCD/CMOS Hybrid FPA for Low Light Level Imaging," in Proceedings of SPIE, 5881, July 2005

[4] B. Fowler and X. Liu, "Charge Transfer Noise in Image Sensors", 2007 International Image Sensor Workshop, Ogunquit, Maine, USA