A 28M 43cm^2 full-frame CCD Imager for Medical and Scientific Applications ("Big is Beautiful")

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INTRODUCTION

Contrary to many consumer applications where cost is a driver for shrinking pixel sizes, certain medical, scientific imaging and aerial reconnaissance applications [1] require large-format imagers. This paper presents a 'half-wafer-scale' 7k x 4k 86mm x 49mm full-frame CCD imager, to our knowledge one of the largest ICs in the world that is in regular production. Next to the challenges in design and wafer fabrication, the paper also describes the solutions for testing, assembly and application development for this very large device.

SENSOR DESIGN

A schematic representation of the sensor is shown in Fig.1. Stitching is used in lithography to manufacture this sensor [2]. The building block concept was presented in [3]. The sensor has 28M 4-phase pixels of 12 x 12μm^2 size, a 3-phase readout register both at the top and bottom, and four identical output amplifiers. Readout can be done through one, two or four outputs by applying the appropriate driving pulses to the horizontal and vertical clocks. To achieve efficient highlight handling, fast electronic shutter and excellent charge transport, a buried channel CCD structure in a p-well on an n-type substrate was chosen [4]. The four-phase bi-directional image section is also beneficial for aerial reconnaissance since it allows a 'TDI'-mode of operation for motion compensation [1].

Special performance challenges relating to very-large imagers had to be met. The first one relates to the RC-time constants of the image electrodes. These 84mm long poly-silicon gates have a resistivity of 35Ω/□. Reducing the resistance by increasing the thickness of the electrodes is no option, since this would decrease the optical transmission. Thus, to achieve a sufficiently high vertical transport frequency, other solutions had to be found. First, etching 'windows' in the pixel area reduced the capacitance of the electrodes, Fig. 2. The reduction in capacitance is larger than the reduction in resistance since a major part of the capacitance is formed by the poly-p$^+$ channel stop capacitance. The capacitance between the electrodes was further reduced by using anisotropic etching for the second poly layer, resulting in adjacent, i.e. non-overlapping electrodes [5].

The holes that are generated in a CCD imager need to be drained efficiently, especially during over-exposure [6]. This means the resistance of the 48mm long p$^+$ channel stops must be small enough to avoid a significant voltage drop. The implant dose was adjusted accordingly.

The doping profiles for the pixel were optimized for operation in "standard mode" (integration with three integrating gates at 8V, blocking gate at 0V; and transport with clock voltages from 0V to 11V) and in "high-charge capacity mode' (integration at 10V and transport at 14V). This required careful optimization to combine good overexposure control with excellent transport efficiency since the risk of charge being trapped at the interface for large charge packets transported increases at 14V [7]. By transporting with externally applied clock voltages larger than the integration voltages, the effective clock swing in the center of the image by the RC time constants is significantly reduced to avoid charge transport problems.

Charge binning is supported; the horizontal and vertical binning ratios can be independently controlled by an appropriate choice of pulse waveforms. Vertical binning is done in the horizontal register and is facilitated by over-dimensioning this register for 2x the maximum charge of the image pixel. Horizontal binning, e.g. 2x, can be achieved by adding charge under the last gate (SG, summing gate) before the output gate or on the floating diffusion, respectively by clocking SG or the reset gate (RG) at half the register frequency. To support the required high charge capacity, SG and RG can be clocked with a 10V clock swing.

SENSOR FABRICATION, TEST AND ASSEMBLY

For an imager in regular production, a predictable, stable and 'high' yield is important. Both the technology and design were optimized for performance as well as for yield. A process using three layers of poly-silicon and one layer of metal is used for manufacturing the sensor. Only 13 mask layers are required. For yield optimization, the minimum feature size used is 0.7μm, while 0.35 μm is technologically possible.
Another aspect of regular production is the fit of the imager design with the parametric test equipment of the wafer fab. By having separate connections for the four quadrants, and by placing all bond pads for the imager present close to the four corners of the design, the sensor parametric test can be performed with 'standard size' probecards on standard parametric test equipment. A +-shaped probecard, common for the whole family of 12 x 12μm^2 pixel-size full-frame imagers, is used to probe four corners of four adjacent devices in a single sequence (Fig. 3).
The sensor is functionally tested on wafer in the assembly clean room at the sensor development site, using a standard wafer prober combined with dedicated optics and electronics. Hermetical sealing in a ceramic package with glass lid without out-gassing problems was achieved by the implementing correct specifications of the package, glass and die and cover glass adhesive, and by a proprietary sealing technique. After assembly, the sensor is fully tested in a dedicated test set up.

SENSOR APPLICATION AND PERFORMANCE

The sensor performance at 20kHz vertical transport and 10MHz horizontal transport is identical to that of smaller devices using the same 'building blocks' [8]. No effect of the imager size is seen on highlight handling or charge transport efficiency. Table 1 shows a performance summary.
The sensor can be operated by existing peripheral circuitry as shown in Fig. 4, thus allowing a compact, 'low-power' application. The power consumption of the sensor itself, when reading 0.25 fps through one amplifier only, and with 11V image clock swing, is only 1.5W, the equivalent of 3W per wafer or 35mW/cm^2, which implies that this device can be considered a true low-power imager…
Table 1 summarizes the performance. Fig. 5 shows two sensors on a 6" wafer after processing, and Fig.6 the assembled sensor. Fig. 7 shows an image obtained with this sensor.

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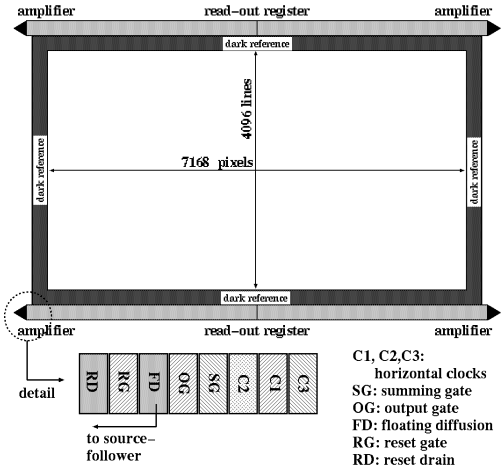

Fig.1. Schematic representation of 43cm^2 CCD imager

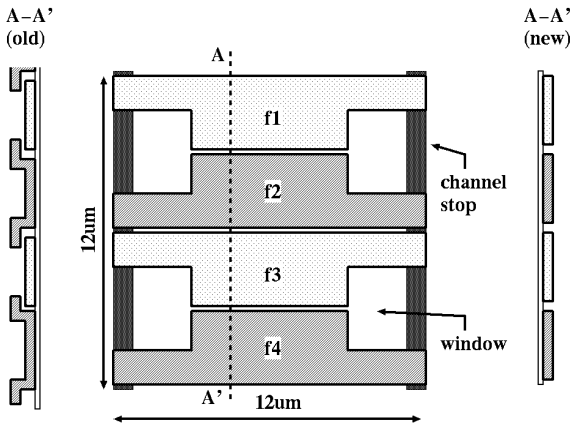

Fig.2. Top view of image pixel and cross-section of electrodes with old (isotropic; left) and new (anisotropic; right) etching method

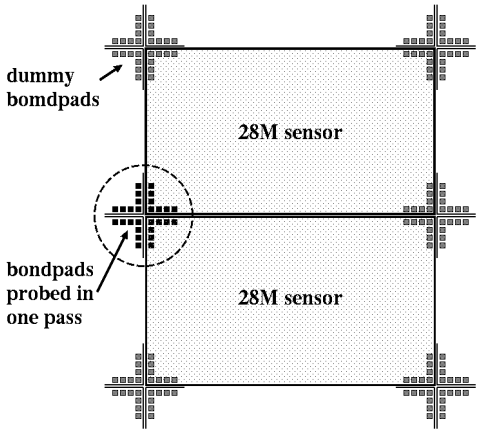

Fig. 3. Parametric probing scheme for 43cm^2 CCD imager

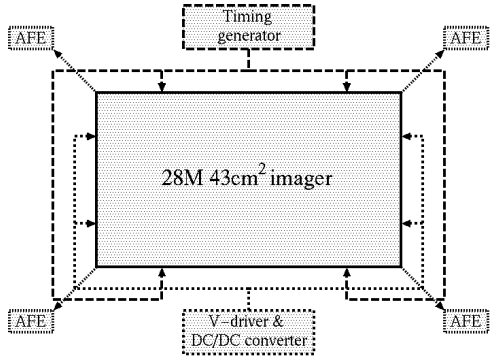

Fig.4. Application schematic. The circuitry is identical to that needed for smaller devices using the same building blocks (AFE: analog front-end with CDS & ADC)

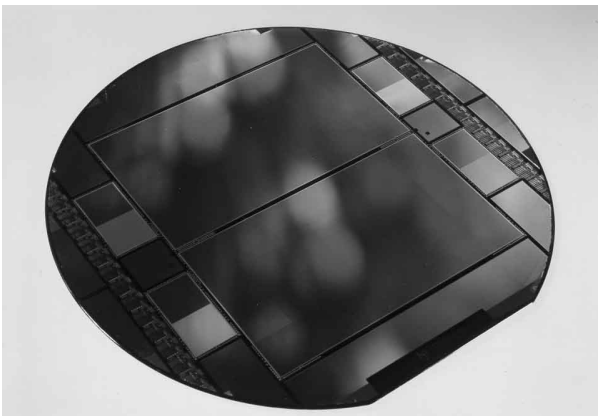

Fig.5. 6" wafer with two 28M 43cm^2 CCD imagers

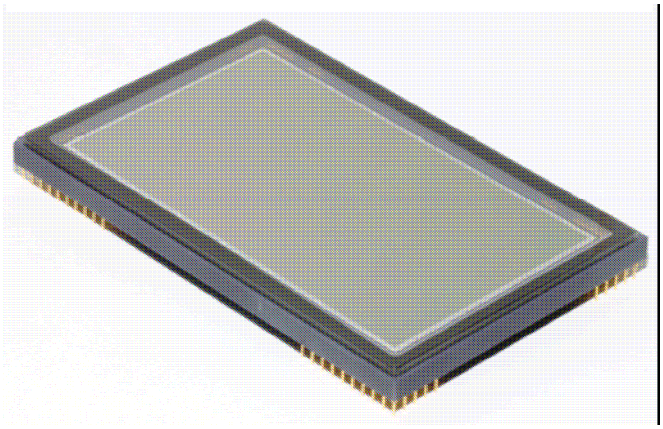

Fig. 6. Assembled sensor in hermetic PGA package

CCD type	Full-frame
Optical size	86mm x 49mm
Chip size	43cm^2
Active area	42cm^2
Resolution	7168 (H) x 4096 (V)
Pixel size	12 x 12 μm^2
Technology	Three poly-silicon layers, one metal layer
Minimum feature size	0.7 μm
Image pixel	Four-phase, bi-directional, 100% fill factor
Image performance	Vertical anti-blooming (200x overexp.), electronic shutter
Readout register	Three-phase, bi-directional
Number of outputs	4
Output amplifier type	Triple source follower, external load for 3rd stage
Output formats	Full resolution & n x m binned
Output mode	Single, dual, quadruple output
Maximum vertical frequency	20kHz
Pixel charge capacity (0V-8V int., 0V-11V transp.)	380,000 electrons
Pixel charge capacity (0V-10V int., 0V-14V transp.)	550,000 electrons
Maximum horizontal frequency	10Mhz
Clocks swing readout register	5V
Charge transport efficiency (H&V)	> 0,999 999 5
Readout register charge capacity	800,000 electrons
Maximum charge capacity (horizontal binning, detection node)	800,000 electrons (10V SG and RG clock swing)
Output amplifier conversion factor	8 μV/e$^-$
Amplifier noise after CDS processing	35 e$^-$
Package	Ceramic, 104-pins PGA with hermetical seal (available also without cover glass)
Flatness	25μm

Table 1. Overview of device specifications

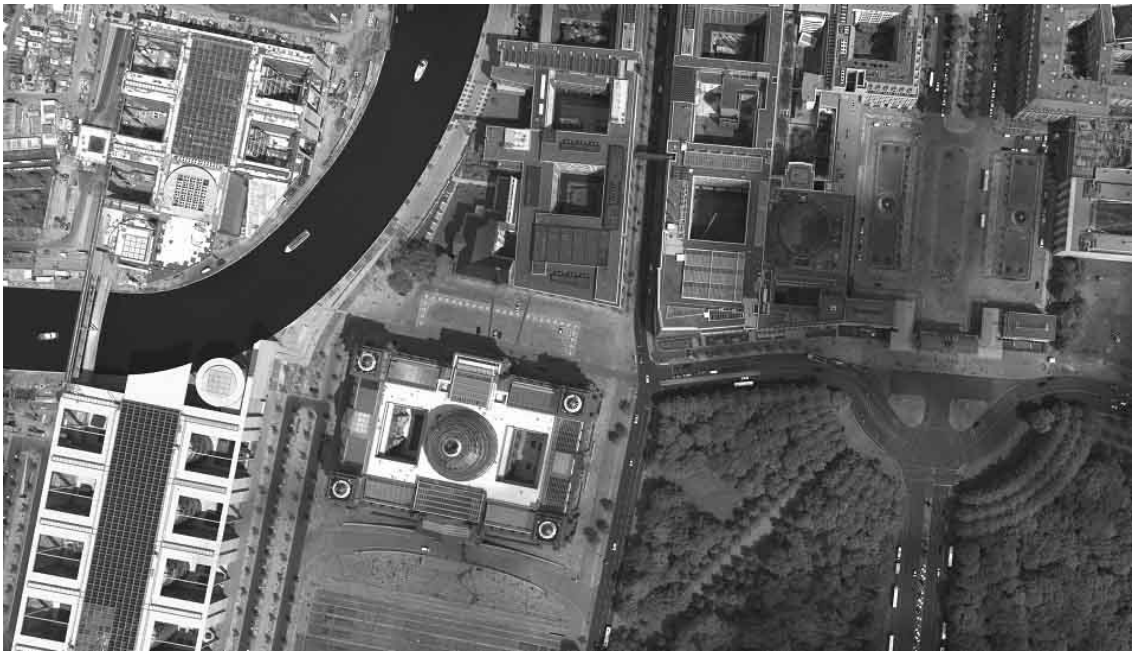

Fig.7. Image obtained with 28M 43cm^2 imager (Reichstag, Berlin)