2MPix 2.6µm Pixel Size Image Sensor in AIC Technology

T. Lulé, F. Mütze, M. Sommer
J. Prima[(1)], F. Roy[(1)], B. Glück[(1)], D. Thomas[(1)], R. Nicol[(2)]

STMicroelectronics, Imaging Division, 12 rue Jules Horowitz,
38019 Grenoble, France, tarek.lule@st.com, +33 4 76 58 59 35
(1) STMicroelectronics, 850 rue J. Monnet, 38926 Crolles Cedex, France
(2) STMicroelectronics, 33 Pinkhill, Edinburgh EH12 7BF, UK

Abstract

The general interest in AIC image sensors lie in the 3D integration that vertically separates light collection and signal processing, naturally giving rise to high QE. Low optical cross-coupling is replaced by an electrical cross coupling that can be mastered with standard CMOS design techniques. A 2MPixel image sensor with 2.6um pixel size is presented with very large full well and good low light sensitivity despite the presence of kTC noise. Permanent change of material characteristics under extreme light conditions has been reduced by optimization of material properties and design paradigms.

Introduction

Various CMOS image sensors overlaid with thin amorphous semiconductor layers, also sometimes referred to as AIC (Above-IC) or TFA (Thin-Film on ASIC) image sensors, have been presented in the past. In some publications the additional layers are used to create avalanche photodiodes that amplify the photo-generated current which can lead to high pixel to pixel gain variations [1]. Instead, the present publication realizes a good sensitivity in low light conditions due to the large quantum efficiency of the amorphous silicon photodiode as was predicted previously [2].

Figure 1 shows the principle cross section of an AIC image sensor. Only the readout electronics is realized by standard bulk CMOS technology. The amorphous silicon layer system is deposited on top of the CMOS wafer. It is sandwiched between two electrodes where the front electrode is realized from a transparent conductive oxide (TCO) while the rear electrode can be realized from any suitable material [3].

Cross-Coupling

In CMOS image sensors, the number of metal layers is strongly limited as the light that passes through the color filter must be focused on the corresponding photo diode. Any reflection, scattering contributes not only to the loss in signal in the targeted pixel, but furthermore when impinging on a neighbor pixel contributes to color cross talk. This cross talk reduces the separation of the colors and needs to be corrected by a color matrix with larger off-diagonal components which reduces the usable signal and adds noise thus reducing the signal to noise ratio twofold [4].

In AIC image sensors, after passing a color filter the light only has to penetrate the TCO electrode and is absorbed directly in the underlying AIC a-Si layers. Effectively the optical path length is greatly reduced. This directly allows for lens designs with much larger chief ray angle as can be found especially in miniature camera modules for portable devices such as mobile phones. Applications with high circuit density or more complex pixel architectures also benefit from the additional routing layers, as for example the 120dB LARS image sensor employing an auto-exposure mode per pixel [5]. Instead, an effect on signal quality is given by capacitive coupling (depicted by symbolic equipotential lines) between adjacent metal lines around the conductors for the photo current, which can be much easier controlled. The optical cross coupling effect when transporting the light through the metal stack in CMOS sensors is thus replaced by an electrical cross coupling effect, both being electromagnetic but at very different frequencies.

Sensor Design

A 2MPixel (1620 x 1228) image sensor with 2.6um pixel size has been realized based on a 180nm technology node with 5 layers of metal. The pixel is based on a commonly used CTIA architecture shown in Figure 2 [6]. While the photodiode is realized in the a-Si:H layers, only three transistors need to find place in the pixel as shown in pixel layout of Figure 3. The largest transistors M1 forms the driver of an inverter. It's large size leads to a reduction in 1/f noise and probability for RTS noise. M1 is connected to a common column line through a read transistor M2. The

input and the output of the CTIA are shorted by the third transistors M3 to reset the pixel to a voltage level depending on M1. The integration capacitor is realized by parasitic metal-metal capacitance throughout the metal stack thus benefiting from the large number of metal layers.

The chip floor plan is shown in Figure 4 with the pixel matrix marked in red. Mainly analogue support circuits have been implemented here as the most critical elements. An I2C interface serves to configure various analogue settings and test modes. Otherwise, the digital control logic is largely implemented in an external FPGA to allow for flexible changes in timing or operating modes. A CDS readout mode with uncorrelated kTC noise is used to reduce FPN while a kTC-noise-correlated mode, called double-read, employs the use of a buffer memory to store an image of the per-pixel kTC noise level.

Results

Figure 3 shows a sample picture taken from the image sensor with an excellent picture quality and no visual artifacts such as pin holes or white pixels. The measured dark current has a mean value that is much higher than for pinned photodiode technology. However, the distribution proves to be more narrow which provides a comparable level of white pixels at low light illuminations.

Feature	Performance
Pixel Size	2.6 µm
Sensitivity @6000K	1.8 V/lxsec
Conversion Gain	88.2 uV/e^-
Max. SNR (incl. FPN)	40 dB (29 dB)
Read Noise (Single Read)	11 e^- (59 e^-)
Dynamic Range (Single Read)	47 dB
Dynamic Range (Double Read)	62 dB
Dark Current Mean/Sigma	49 aA / 26 aA
Min. Illumin. @T=67ms,DblRd	22 mlx
Full usable Well	13.8 k e^-
FPN	680uV
Pixel PRNU at Sat. (T=67ms)	1.8%

Table 1 Performance Characteristics of AIC Image Sensor

The detailed performance characteristics in Table 1 show the typical features of a CTIA pixel design. The small effective integration capacitance leads to a high sensitivity in V/lxsec.

The concomitant large kTC noise needs to be corrected by means such as double read operation, in order to provide good low minimum illumination value of 22mlux. As can be shown, the kTC noise can become progressively de-correlated between start and end of frame for long frame lengths, given and depending on the a-Si coupling resistance between adjacent pixels. A tapered reset analogue to previous proposals [7] theoretically giving a reduction of kTC noise level by nearly 2.5, was shown to be difficult to apply due to inherent variations of Vth of the reset transistor M3.

When focusing strong light sources (Halogen bulb, Sun) the lens creates a very high intensity light spot on the sensor surface of up to 100Mlux. The extreme light condition can lead to change in the properties of the amorphous material called “aging” as was discussed in previous publications [8].

The two effects that produce at first are a reduction in sensitivity and an increase in dark current. The stability under these conditions was greatly improved based on circuit and technology efforts [9]. As a novel approach to the effect, a safe operating area in the intensity/time space has been defined as the operation condition under which no visual artifacts due to this effect is noticeable. Figure 6 shows the safe operating area chart that was obtained from the sensor using state of the art AIC technology. The points follow an $I^2 \times T = \text{const}$ trend line rather than $I \times T = c$.

Outlook

Figure 7 shows a sample 1.39um pixel in AIC technology using a 3T source follower architecture per pixel based on a 130nm technology node with little process modifications. Using parasitic extraction programs and ELDO simulator the performance of the pixel is extrapolated. While the full well and maximum SNR are still large with >11ke and 40dB, the dynamic range is clearly limited by the kTC noise of the diode and wiring capacitance to 50dB. The demand of the kTC-correcting double read of a frame store becomes more and more common in today applications. Alternative techniques that compensate for at least part of the kTC noise have been published previously and would allow to regain a dynamic range of 60dB.

Acknowledgements

The authors would like to thank all actual and former colleagues of ST France and UK, as well as from CEA/LETI and UNAXIS who have contributed to the results.

References

[1] Y. Takiguchi et al, IEEE Trans. on Electron Devices, Vol. 44, No. 10, p. 1783, 1997

[2] T. Lulé et al, IEEE Trans. Electron Devices, vol. 47, p.2110, Nov. 2000

[3] M. Böhm et al., Materials Research Society Symposium Proceedings, Vol. 507, p. 327, 1998

[4] R. Nicol et al., 2005 IEEE Workshop on CCD and Advanced Image Sensors, p. 84

[5] T. Lulé et al., 1999 IEEE Workshop on CCD and Advanced Image Sensors, p. 215

[6] Fowler et al, Sensors and Camera Systems for Scientific, Industrial and Digital Photography. Applications II, Proc. SPIE Vol. 4306, p. 68, 2001

[7] B. Pain et al, 1999 IEEE Workshop on CCD and Advanced Image Sensors, p. 140

[8] R. Miyagawa, IEEE Trans. on Electron Devices, Vol. 39, No. 2, p. 325, 1992

[9] N. Moussy et al, IEDM Technical Digest, p. 182, 2006

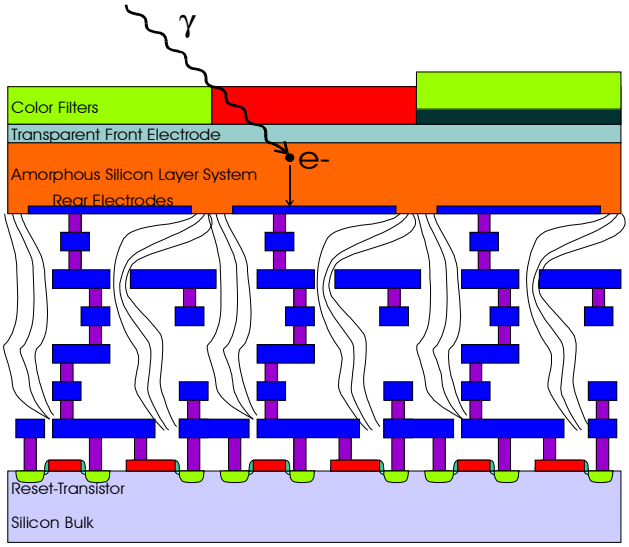

Figure 1 Principle Cross Section of AIC Image Sensor Technology

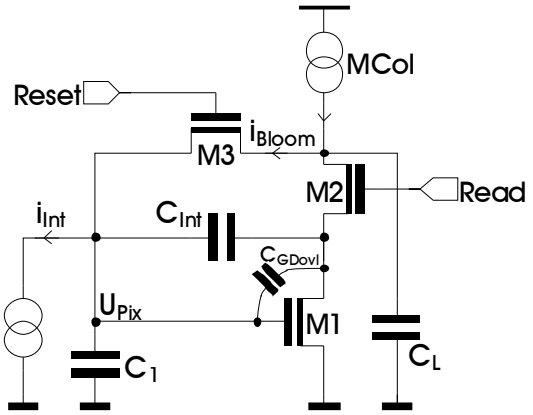

Figure 2 Schematic of CTIA Pixel Architecture of the AIC Image Sensor

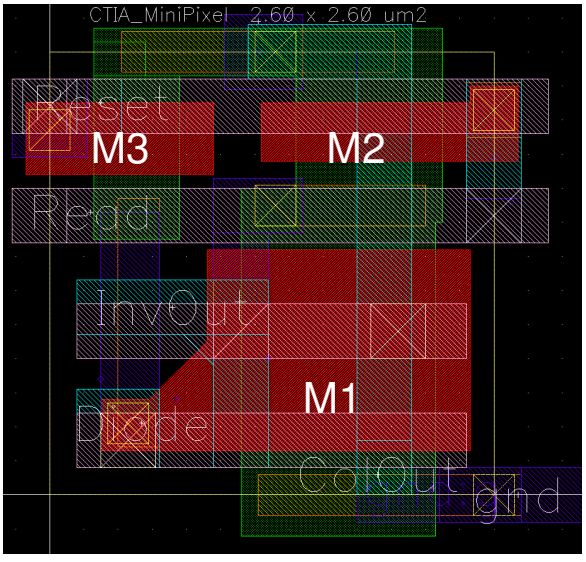

Figure 3 Layout of CTIA CMOS Pixel Circuit

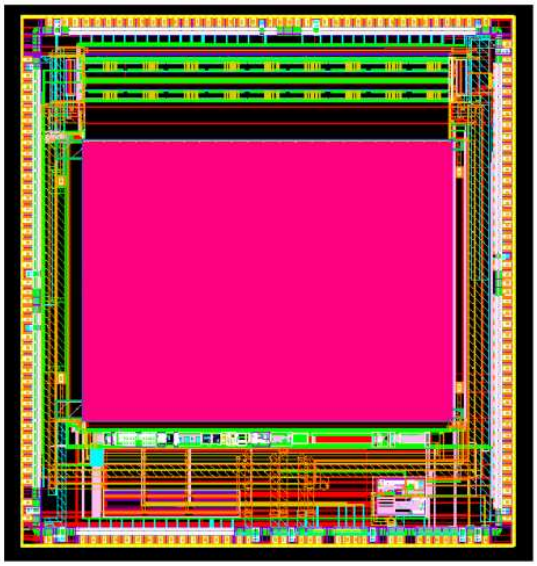

Figure 4 Chip Layout of 2MPix Image Sensor in AIC Technology

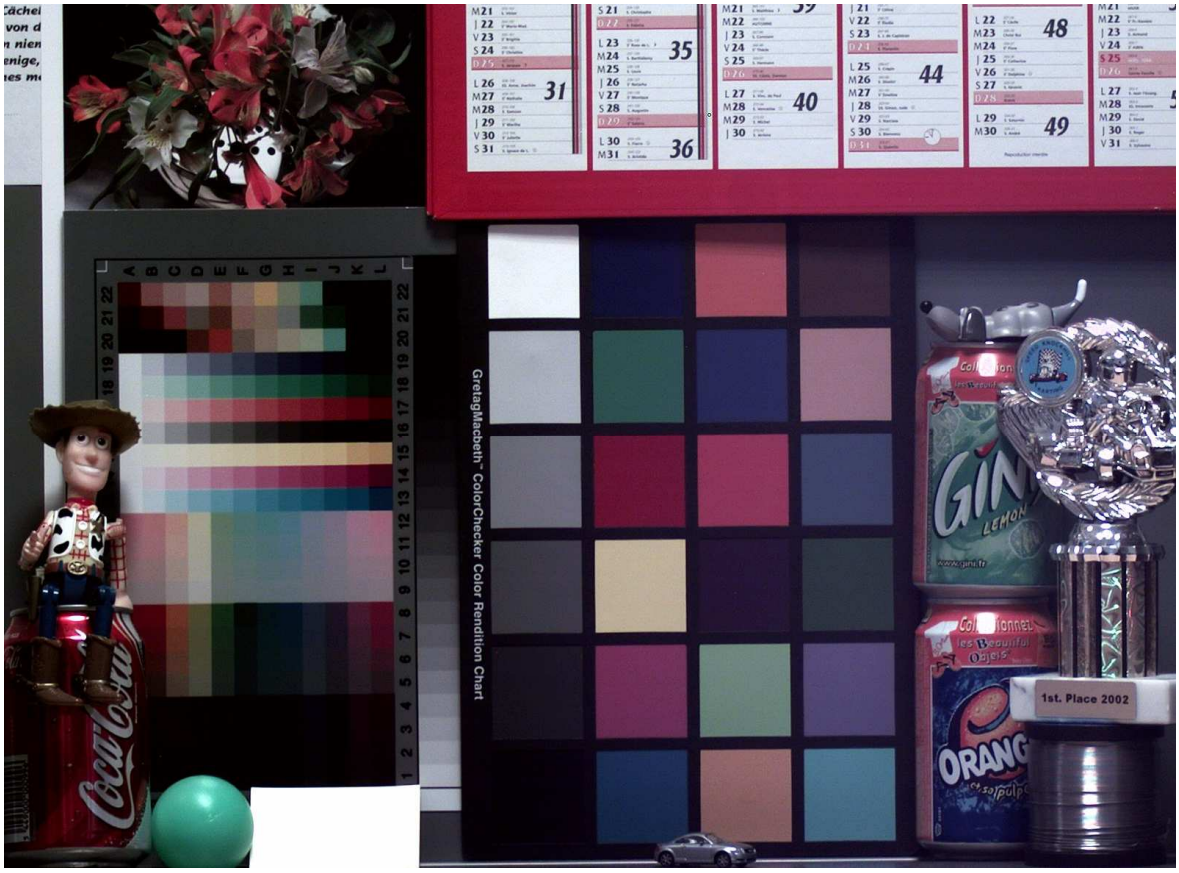

Figure 5 Color Picture Taken with the Sensor

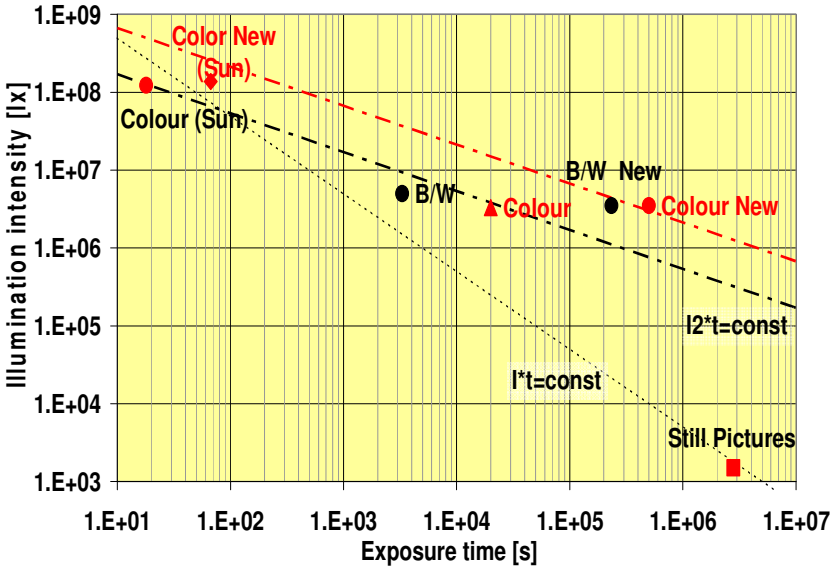

Figure 6 Safe Operating Area Chart for AIC Image Sensor for initial and Improved (New) Sensors with (Color) and without (BW) Color Filters

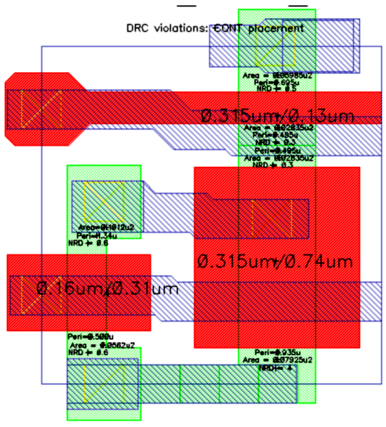

Figure 7 Sample 1.39um Pixel in "130nm based Technology"