

# A CMOS Single-Photon Avalanche Diode Sensor for Fluorescence Lifetime Imaging

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**Abstract** — This contribute describes the design and preliminary characterization of a 16x16-pixel array based on Single Photon Avalanche Diodes (SPADs), fabricated in a standard high-voltage 0.35 $\mu\text{m}$  CMOS technology, and aimed at the analysis of fluorescence phenomena. Each pixel integrates a SPAD combined with an active quenching circuit and a voltage comparator for the digital conversion of the avalanche event. The sensor features a minimum detectable photon density of  $10^8$  photons/cm<sup>2</sup>s, with a maximum dynamic range of over 120dB. Detection of fluorescence light has been demonstrated with a 160ps time resolution over a 100ns observation window.

## I. INTRODUCTION

We have assisted, recently, to a growing interest in fast, portable and low-cost biological test equipment. However, existing systems are aimed at research applications mainly, featuring excellent performance but not suitable to be used in handling, self-test diagnostics. Among the many methods used for biological testing, optical detection is the most common. In particular, fluorescence lifetime imaging is an investigation tool of paramount importance in molecular biology and medicine, allowing the mapping of many cell parameters and the detection of pathologies or DNA sequencing [1]. A typical fluorescence lifetime experiment [2] uses a pulsed or modulated laser to excite the fluorescent markers (fluorophores) and the emitted light is revealed by means of intensified CCD cameras or photomultiplier tubes [3] in order to achieve the required time-resolution and light sensitivity. The performance of these laboratory instruments is excellent but they are expensive and bulky. On the contrary, high accuracy time resolution can be achieved exploiting SPADs. The feasibility of SPADs in conventional CMOS technology, as recently demonstrated [4]-[10], opens the way to the realization of low-cost and high-performance fully integrated systems for high sensitivity imaging.

In this paper we propose the integration, at the pixel level, of a SPAD, an active quenching circuit and a voltage comparator for the digital conversion of the detected photon. The pixel array can be addressed using different operation modes which allow using of the sensor for various applications (2D imaging, 2D phase-imaging, single-point range finder, Time-Correlated-Single-Photon-Counting).

To validate the operation principle, a test chip consisting of a 16x16-pixel array has been fabricated in a HV 0.35- $\mu\text{m}$  CMOS technology. The sensor features a minimum detectable photon density of  $10^8$  photons/cm<sup>2</sup>s, with a maximum dynamic range of over 120dB. Time-resolved measurements of fluorescence light have been successfully demonstrated. In the following sections, the pixel read-out circuit will be described, the overall chip architecture and the SPAD characteristics will be presented and selected experimental results will be shown.

## II. MEASURING TECHNIQUE

The adopted measuring technique, based on a time-gated detection method and the system setup are sketched in Fig. 1.

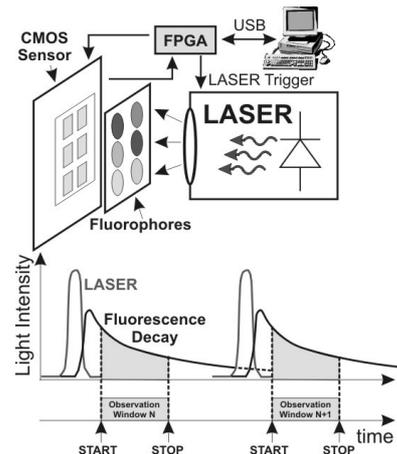


Figure 1: System setup and measuring technique.

An FPGA module, interfaced to a PC via USB, provides all the digital control signals required by the sensor and triggers a pulsed laser (FWHM=80ps) which illuminates the biological sample containing the fluorophores. The adopted measuring technique is based on a time-gated detection method, where the light signal is detected by using two or more observation windows. Each window has an externally programmable time width and can be delayed with respect to the trigger of the laser pulse by a user-defined time value. The time offset between the laser pulse and the beginning of the observation window offers the possibility of suppressing unwanted background signals like scattering and auto-fluorescence. This improves the signal-to-background ratio when the light intensity is measured.

The measurement starts setting the first observation window synchronized with the laser trigger. If an avalanche event is generated within this window it will be detected by the in-pixel event counter. The measurement is then repeated for a programmable number of times ( $N_p$ ) so that a significant statistical population can be obtained. After that, other  $N_p$  measurement cycles are performed by using time delayed observation windows. At the end of the full measurement it is possible to sketch a histogram reporting the number of detected events within each observation window.

### III. PIXEL ARCHITECTURE

The schematic cross section of the implemented SPAD and the pixel circuit schematic are shown in Fig. 2. The pixel consists of a SPAD, a reset transistor  $M_{p1}$ , a voltage comparator (INV1) for the avalanche event detection and a voltage buffer (BU1) for the 5V-to-3.3V conversion.

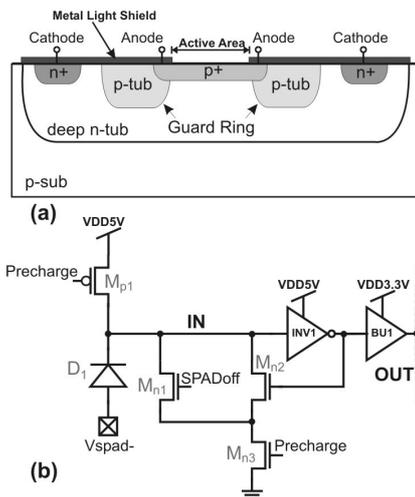


Figure 2: (a) SPAD cross-section and (b) pixel schematic.

The geometry of the SPAD is square to optimize the area occupation, but the corners are smoothed so as to avoid electric field peaks at the junction corners.

Edge breakdown is prevented by means of a guard-ring surrounding the p+ implantation obtained using the special

p-tub layer which is available inside a deep n-tub in high voltage processes.

The active area is defined by means of an optical window opened in the metal light shield only in correspondence with the region where avalanche multiplication occurs.

The cathode of the SPAD is connected through an active recharging circuit to VDD5V, and the biasing above the breakdown voltage  $|V_b| \approx 28$  V of the SPAD is assured by means of the external line  $V_{spad-}$  biased at a very negative voltage.

The feedback loop, consisting of INV1 and  $M_{n2}$ , realizes an active quenching mechanism, able to force the input node to ground as soon as an avalanche event is detected. In so doing only the first avalanche event is detected while rejecting possible after-pulses. At each clock cycle an active low Precharge pulse biases the SPAD in the breakdown region so that the detector is ready to detect photons. Each observation window starts at this moment (OUT is pulled down by the voltage comparator). When a photon is absorbed by the SPAD, the avalanche is triggered and the node OUT is pulled up.

### IV. CHIP DESIGN AND ARCHITECTURE

The overall chip architecture is sketched in Fig. 3.

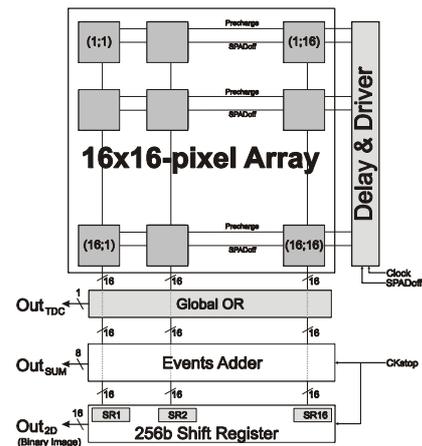


Figure 3: Sensor architecture.

The 16x16-pixel array can be addressed by using three different operation modes externally set up by the user:

- 2D-mode: at the end of the observation window (rising edge of the Ckstop signal), each pixel can be read out serially by means of the 256b shift register to obtain a binary image at each measurement cycle ( $Out_{2D}$ ).
- 1D-mode: as an alternative, the pixel array can operate as a single big-pixel, simply adding together all the events obtained from each single pixel ( $Out_{SUM}$ ).
- TCSPC-mode: with a logical OR operation of all the pixel outputs ( $Out_{TDC}$ ), it is possible to identify the

first avalanche event and use its arrival time information with an external time to digital converter, in order to obtain a Time Correlated Single Photon Counting (TCSPC) measurement.

The microphotograph of the fabricated sensor, where the main functional blocks have been evidenced, is shown in Fig. 4.

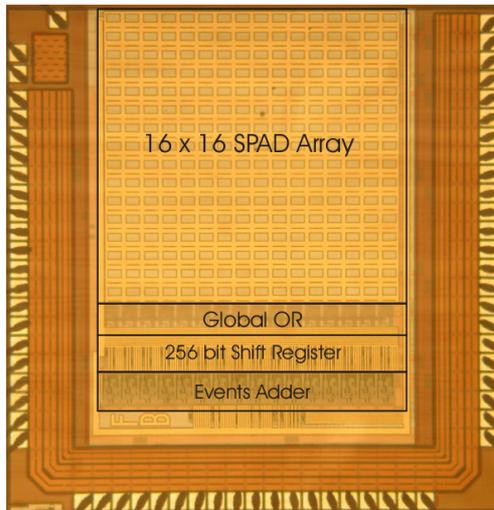


Figure 4: Chip micrograph.

## V. EXPERIMENTAL RESULTS

Preliminary experimental results, as obtained from electro-optical characterization of on-chip test structures, are summarized hereafter. The SPAD dark count, as obtained from a  $20 \times 20 \mu\text{m}^2$  test structure at room temperature, is shown in Fig. 5, while Fig. 6 reports the measured spectral dependence of Photon Detection Probability (PDP).

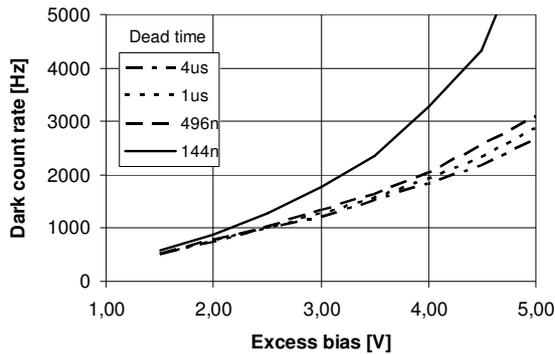


Figure 5: SPAD dark count as a function of the bias voltage and for different dead time values.

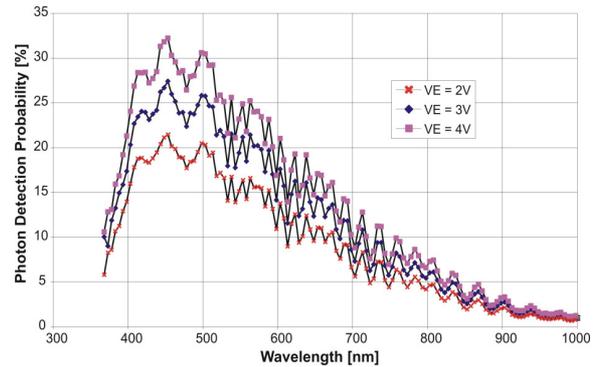


Figure 6: SPAD Photon Detection Probability for different values of the excess bias voltage.

A characterization of the number of counts as a function of optical power density has been performed on a dedicated electro-optical bench (see Fig. 7), demonstrating the high dynamic range capability of the proposed sensor.

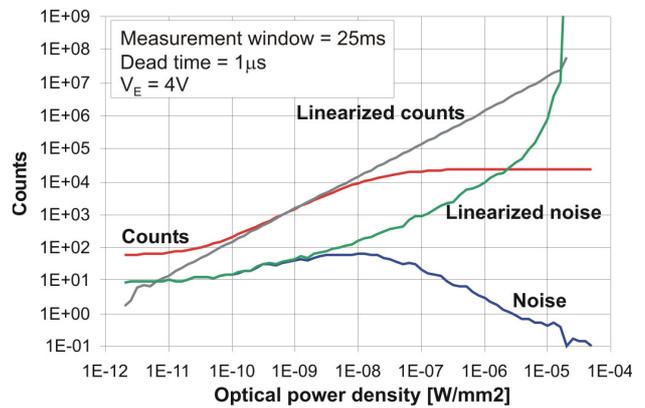


Figure 7: Sensor power responsivity curve. The number of signal counts and noise are shown.

The timing resolution has been measured using a pulsed semiconductor laser ( $\lambda=480\text{nm}$ ) with 80ps pulse width and a TCSPC instrument. The resolution measured on a  $20\text{-}\mu\text{m}$  SPAD at 5V excess bias is 160ps FWHM and 550ps FWHM/100 (**Error! Reference source not found.**).

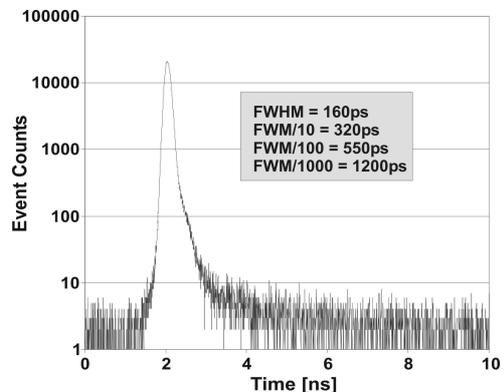
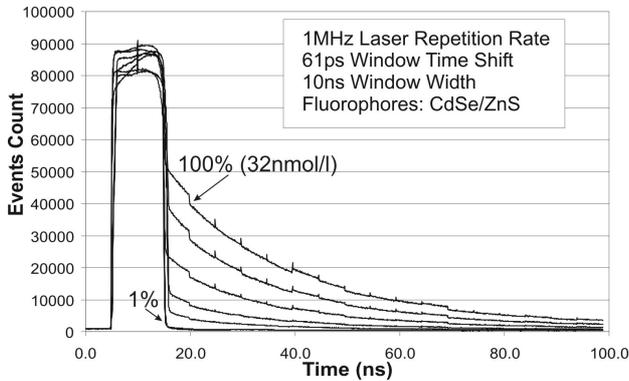


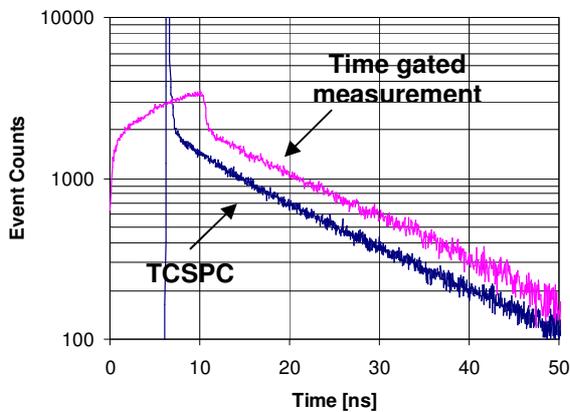
Figure 8: System time resolution.

Finally, the measurement of fluorescence decay curves, as obtained from a CdSe/ZnS quantum dot fluorophores (Evident Technologies), considering different sample concentrations is shown in Fig. 9. For this measurement the observation windows width is 10ns and the time shift is 61ps.



**Figure 9: Measurement of fluorescence decay curves with different sample concentrations.**

To prove the validity of the proposed approach, a comparative measurement of fluorescence decay obtained with our sensor, using internal time-gated detection, and coupled to a commercial TCSPC module (PicoQuant PicoHarp 300) is shown in Fig. 10.



**Figure 10: Comparative measurement of fluorescence decay with our sensor using internal time-gated detection and coupled to a commercial TCSPC module (PicoQuant PicoHarp 300).**

The main chip characteristics are summarized in Table I.

TABLE I. PERFORMANCE OF THE DEVELOPED SPAD SENSOR.

|                  |                                    |
|------------------|------------------------------------|
| Technology       | 0.35 $\mu$ m, 3.3V HV CMOS (2P-4M) |
| Pixel dimensions | 100 $\mu$ m $\times$ 100 $\mu$ m   |
| Fill factor      | 30%                                |
| Array size       | 16x16-pixel                        |
| Die size         | 2.660 x 2.740 mm <sup>2</sup>      |

## VI. CONCLUSIONS

A pixel architecture implementing a SPAD detector and dedicated read out circuitry for fluorescence lifetime measurements has been presented. Each pixel allows for single photon detection and measures the number of events generated within a user-defined observation window. A preliminary test-chip, consisting of a 16x16-pixel array, has been fabricated in a high-voltage 0.35- $\mu$ m CMOS technology allowing the measurement of photon densities as low as 10<sup>8</sup> photons/cm<sup>2</sup>s. Time-resolved measurements has been demonstrated by detecting fluorescence decay curve of commercially available reference fluorophores.

## ACKNOWLEDGMENT

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