

Evaluation of a Small Negative Transfer Gate Bias on the Performance of 4T CMOS Image Sensor Pixels.

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I. Introduction.

From the early development of Virtual Phase CCD Image sensors it became well known that the negative bias applied to the CCD gates results in accumulation of holes at the interface^[1,2]. This leads to quenching of the interface states at the Si-SiO₂ interface under the poly-silicon gates and a significant reduction of dark current. In modern 4T CMOS image sensors the similar effect is typically accomplished by placing a suitable p-type doping implant under the transfer gate of the pixel. However, due to very thin gate oxides, which are typically used in today's CMOS image sensors; it is not possible to completely saturate the interface states with holes by using only the implants, since undesirable problems such as the large threshold voltage shift result. For this reason other methods have been developed and are typically used. This paper presents evaluation of application of a small negative bias to the transfer gate of a high performance CMOS image sensor pixel as one possible solution to the problem. The small negative gate bias is easily generated on chip without any difficulty by using simple negative charge pump circuits. A suggested circuit block diagram for the generation of the suitable negative bias on-chip is also shown for completeness. This paper presents data of the negative charge pump effects on the dark current, dynamic range and blooming characteristics. The tested 2 Megapixel imager has 2.2um x 2.2um 2T pixels and

operates with 2.8V analog drain bias as is typical in mobile applications. The negative charge pump circuit can provide bias from 0.0V to -0.5V.

II. Motivation for using the negative charge pump.

During formation of pinned photo diode to minimize the dark current, a suitable p-type doping implant is also used under the gate of the charge transfer transistor in order to fill the interface states with holes in this region. The interface potential should be kept close to 0V. However due to the N+ doped poly-silicon gate typically used for this transistor a built in potential difference of approximately $E_c - E_v$ is applied through a very thin gate oxide to this region. As a result a small potential bending occurs at the silicon surface, leading to the depopulation of the interface states of holes and generation of the dark current. Fig.1.0 shows the drawing of the approximate potential profile under the gate. To achieve a flat band condition and repopulation of the interface states by holes and consequently the dark current reduction a negative charge pump is used to apply a small negative bias to the gate.

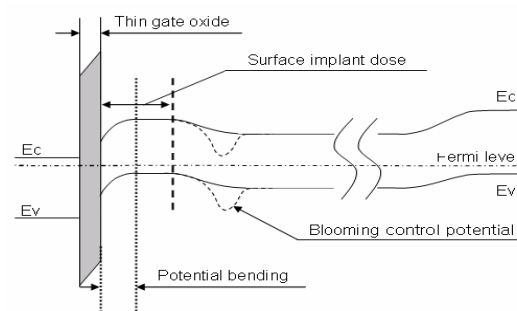


Fig.1.0. Energy band diagram under the charge transfer transistor.

In the CMOS image sensor it is also necessary to take care of the charge overflow to neighboring pixels called blooming. To prevent the blooming effects several approaches are usually used one of them being, for example, a blooming control implant. A dotted line

in Fig.1.0 indicates the energy band diagram where the implant was used. When the negative charge pump is turned on, the potential profile shouldn't significantly change in order to maintain a good blooming control. For a better understanding of the device structure Fig.1.1 shows the drawing of the device cross section under the transfer gate region.

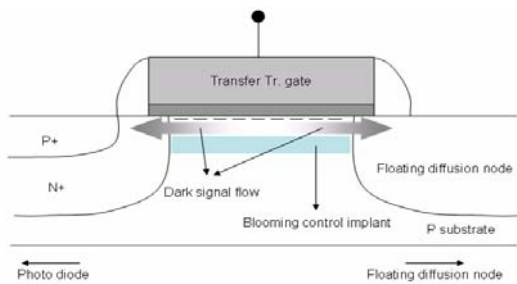


Fig.1.1. Cross section of the transfer gate region showing the interface states generated dark current flow and the blooming control implant location.

A portion of the interface states generated dark current flows into the floating diffusion and remainder flows into the photo diode. When the charge transfer transistor is turned off and a negative bias is applied to the gate holes are accumulated at the interface. This results in a significant reduction of dark current generation. Fig.1.2 shows the block diagram of the on chip negative charge pump circuit.

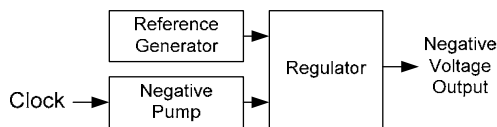


Fig.1.2. Block diagram of on chip negative charge pump circuit.

The circuit consists of the reference generator, negative bias charge pumping circuit and a regulator. The output is used as a ground level V_{ss} -bias of the transfer gate driver-buffer. The resulting low level voltage applied to the gate of the transfer transistor thus becomes negative. The negative voltage range, which

the circuit can generate, is from 0V to -0.5V with 0.05V steps.

III. Measurements and results.

Fig.1.3 shows the dark current measurement results. The dark current decreases with the negative charge pump bias. When the bias of -0.5V was applied to the gate, the dark current decreases as much as 37% in comparison to the 0V bias. However at the -0.05V bias a small increase has been noticed, which is not fully understood at this time and is currently being investigated.

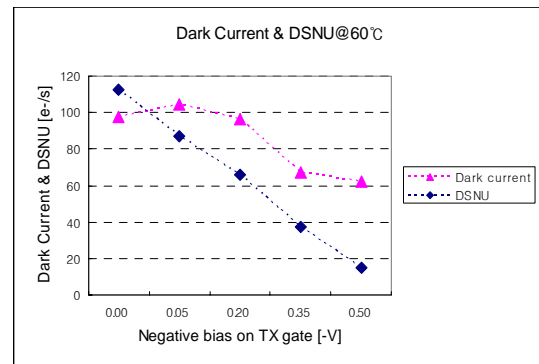


Fig.1.3. Dark current trend as function of the negative charge pump voltage.

Fig.1.4 shows the graph of the dynamic range as function of the negative charge pump bias.

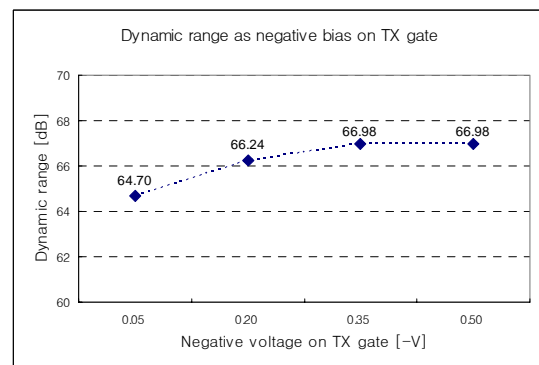


Fig.1.4. Dynamic Range as function of the negative charge pump voltage.

Since the blooming potential level can be affected by the negative gate bias it is necessary to confirm the

blooming performance of the pixel. This is shown in the photographs in Fig.1.5.

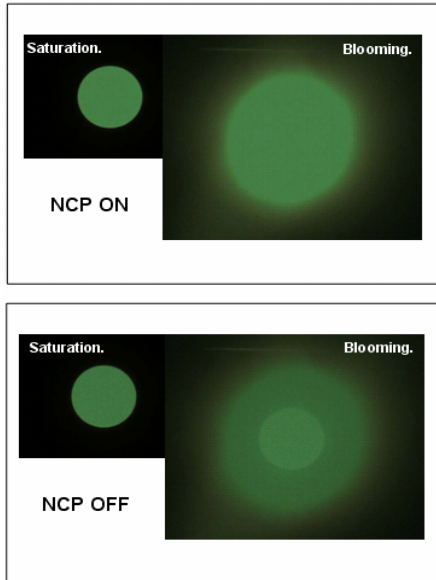


Fig.1.5. blooming image as function of the negative charge pump ON & OFF

An optical fiber was used as a light source for the generation of regular pattern and a module lens was used for the focused image. In case of the negative charge pump being turned off, the light pattern is noticed. The wider spot corresponds to bloomed area. When a lower light intensity is used no blooming pattern is found. With high intensity illumination the image intensity graph shown in Fig.1.6 is measured.

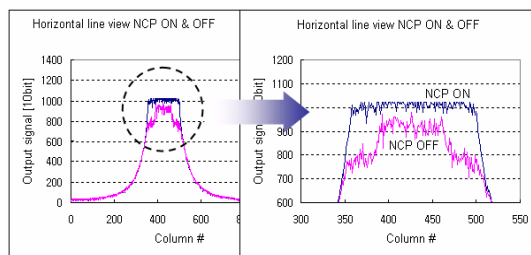


Fig 1.6. Blooming image horizontal view.

When a negative charge pump is turned off the pixel charge output is smaller than the full allowable

analog swing voltage of the ADC converter. When the negative charge pump is turned on the blooming pattern could not be clearly recognized due the signal clipping by the ADC. However, when these two graphs are compared the over all shape of the graphs did not change only the output signal has increased. Fig.1.6 is showing the intensity graphs of the horizontal cross section of image in Fig.1.5. For the case of the negative charge pump turned off the signal is clipped off and only the blooming region remains. Concluding from the results shown in Fig.1.5 and Fig.1.6 it can be stated that the blooming control is working correctly. This means that the negative charge pump bias did not significantly affect the potential profile under the transfer gate.

IV. Conclusions

In this paper the effect of a small negative bias of the charge transfer gate on the CMOS sensor performance was evaluated. It was found that a small bias generated by the negative charge pump is useful for decreasing the dark current and increasing the sensor dynamic range. By using the negative charge pump, the blooming barrier was slightly lowered but the blooming characteristic was not significantly changed. The negative charge pump worked up to -0.5V and it showed approximately 37% decrease in dark signal and 0.24V increase of the saturation level.

Acknowledgements:

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References:

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