Optimization of Random Telegraph Noise Non Uniformity in a CMOS Pixel with a pinned-photodiode

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The main advantage of a 4T CMOS pixel (Figure 1a) which incorporates a pinned PD is the low reset noise and ultra low Dark Current (DC). In principle when the transfer of electrons from the PD to the FD is fully optimized, the reset noise can be eliminated completely by the Correlated Double Sampling (CDS) of the Reset and Signal (Figure1b). Moreover, by proper optimization of the diode and Transfer Gate the DC and DC distribution can be reduced significantly. In this case the limiting factor to the image quality in low light becomes the temporal noise associated with the Source Follower (SF) Transistor[1].

In fact, in state of the art sensors the mean value of the SF temporal noise is inherently low enough due to band-pass filter imposed by the CDS operation [2]. The main limit for good image quality in low illumination becomes the non-uniformity associated with this noise. In Figure 2 the cumulative population of two different arrays (each array contains 480x640 2.2um pixels). The first array contains pixel with optimized SF and the second array pixel with standard SF. It can be seen that while both arrays has similar mean temporal noise well below 10e, the distribution (noise non-uniformity) is completely different: for the optimized SF array only 1% of pixels has temporal noise >10e whereas for the STD SF array 10% of the pixels has temporal noise >15e. The wide distribution of temporal noise causes two main problems: in low illumination condition (assuming low dark current as shown in Figure2) it will set a limit for the maximum analog gain which can be applied to the picture before it becomes grainy; in video applications even at high illumination it will cause some pixel to blink in the darker area of the picture.

In order to reveal the nature of this temporal noise non-uniformity and optimize our process and pixel layout we designed an engineering VGA array with 4um pitch. With this array along with is peripheral test board we could measure temporal noise as low as 150uV. Other features for this engineering array where complete control on pixel timing and voltages. For example one can choose quite simply not to open the TG in the read sequence. In that case the CDS operation should result zero with the uncorrelated SF noise; i.e. with this special timing we could distinguish between noise coming from incomplete transfer to the noise coming from the SF.

Several pixels with different designs for their SF where placed on the engineering VGA array in smaller mini-arrays of 150x150 pixels. In Figure 3, the cumulative plots for the temporal noise of three different mini-arrays are shown. The only change between the pixels is the size of SF transistor channel: pixel (a) has W/L of 0.4/0.4 pixel (b) has W/L of 0.8/0.4 and pixel (c) has W/L of 0.4/0.8. The inner frame in figure three shows time distribution histogram of two individual pixels from the miniarray with pixel (a). The dotted line represent "quiet" pixel – pixel which his noise pattern is similar to 90% of array population. The bold line represent "noisy" pixel – pixel which only 0.1% of the population is similar or worse. The "quiet" pixel is clearly showing one main value with some distribution around it. This noise pattern is typical to

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standard 1/f and temporal noise of a SF transistor under CDS operation [3]. However it is clearly seen that the noisy pixel is going through three different values. The right and left peaks are separated by the same voltage from the central peak. This is the main characteristic of a Random Telegraph Noise with one trap [4]. The magnitude of the noise – distance between peaks depends on the distance of the trap from the source of the SF (closest to the source highest magnitude). The time constant associated with this noise is in the order of usec or less which indicates low activation energy or very shallow traps.

Returning to cumulative plots of Figure 3, we can see that the number of "noisy" pixels strongly dependent on the SF dimensions. Pixel (b) and pixel (c) has the same area but different W/L however there noise performances are quite different. The number of "noisy" pixels is dramatically reduced when comparing pixel (c) to pixel (b) and (a). Thus the most effective parameter (in a given process) for reducing the number of "noisy" pixels is making the SF longer. This phenomenon can be explained by the segregation of the channel implant (Boron) into the Shallow Trench Isolation (STI) walls which is making the threshold voltage near walls smaller than the threshold voltage at the middle of the channel. This enforces most of the SF current to flow in the vicinity of the interface between the STI walls and transistor gate oxide. Most of the low activation energy (short life time) are located along this interface and the probability to find only one trap is decreasing with channel length.

Finally the importance of the delay between reset read and signal read (designated by τ at Figure 1b) is emphasized by comparing the noise pattern of the two lines plotted for pixel (c) on Figure 3. The bold line is taken with τ=6usec and the dashed line is taken with τ=100usec. It can be seen that increasing τ, increases the temporal noise of all pixels. However the number of "noisy" pixels increases more significantly due to activation of different traps which where masked by the CDS operation for shorter τ.

In this paper we have shown that noise characteristics across the array are very different between "quiet pixels" (mean <10e) and noisy ones. Furthermore it is shown that while the "quiet pixels" exhibit regular 1/f noise typical to small transistors in modern CMOS technology, the "noisy pixels" exhibit Random Telegraph Noise (RTN) pattern with very short time constant. It is shown that for a given process conditions the main parameter for improving the array RTN non uniformity is the channel length of the SF. It is claimed that the single trap responsible for the traping-detraping process is located near the edge defined by the SF active channel, the transistor gate oxide and the shallow trench isolation along the SF.

References

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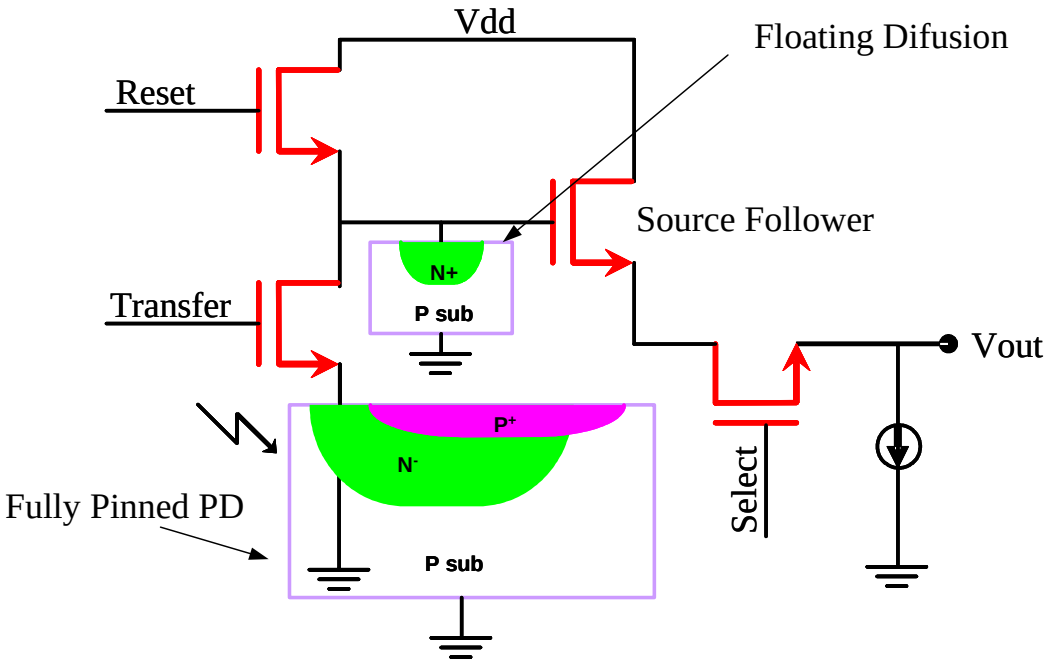

Figure 1(a) – Schematics of a 4T pixel with a fully pinned Photo Diode

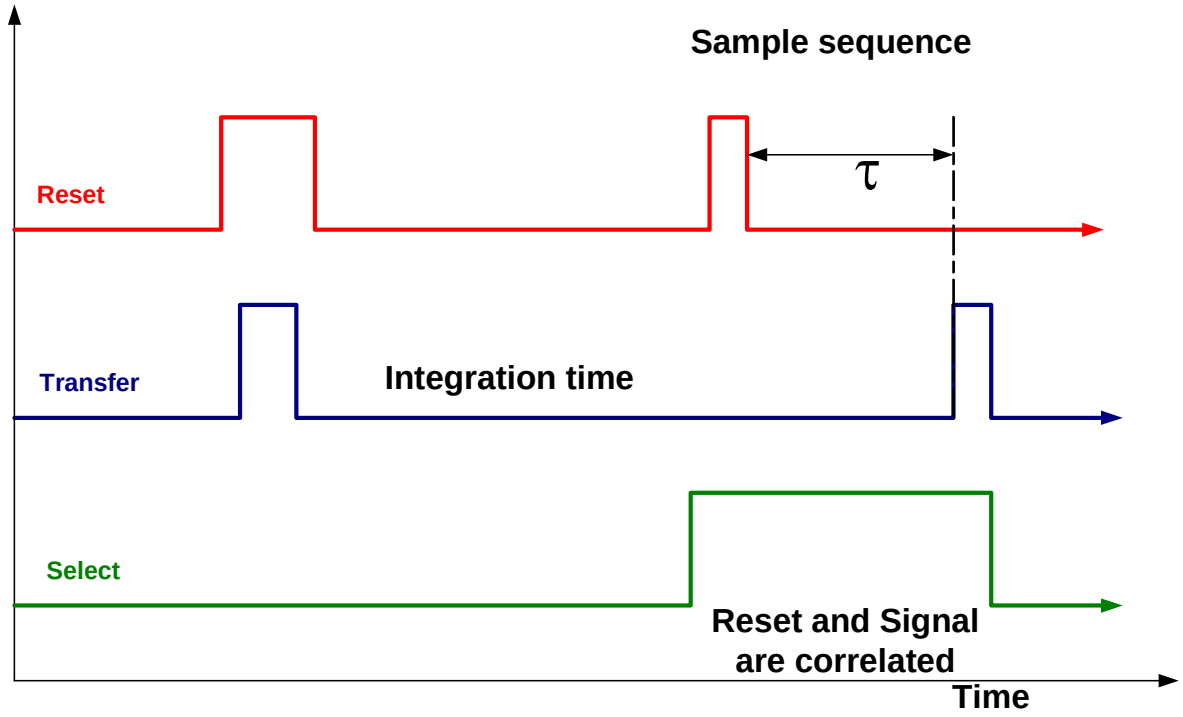

Figure 1(b) – Schematics of a double correlated sampling sequence for a 4T pixel with a fully pinned Photo Diode

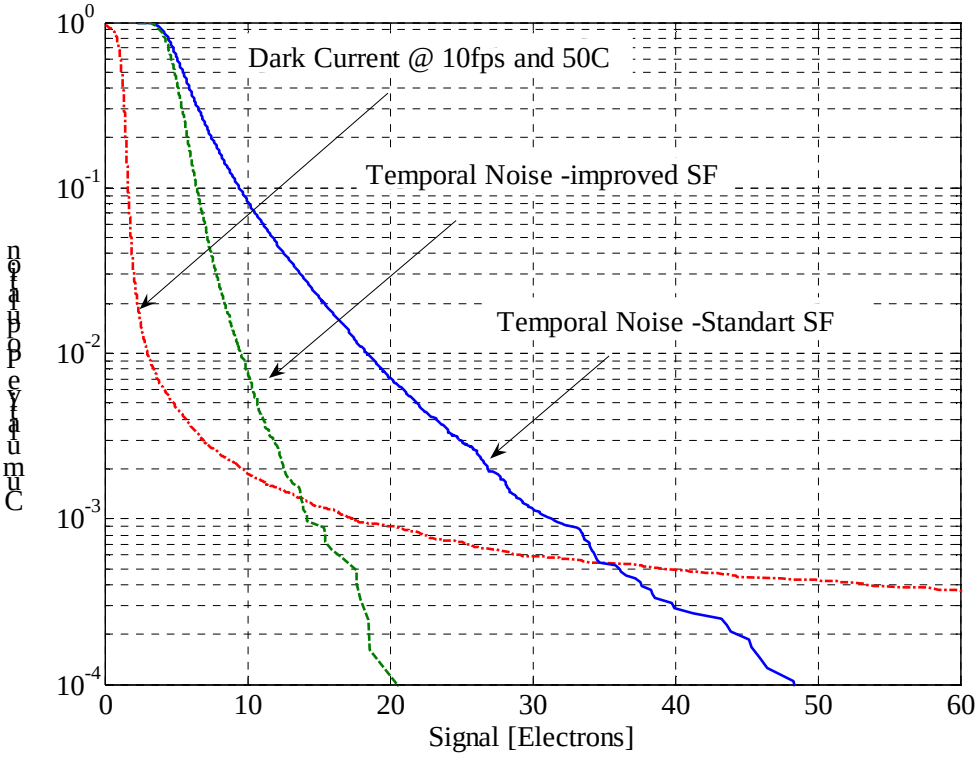

Figure 2 - Distribution of the Dark Current and Temporal noise across a 2.2um pixel array.

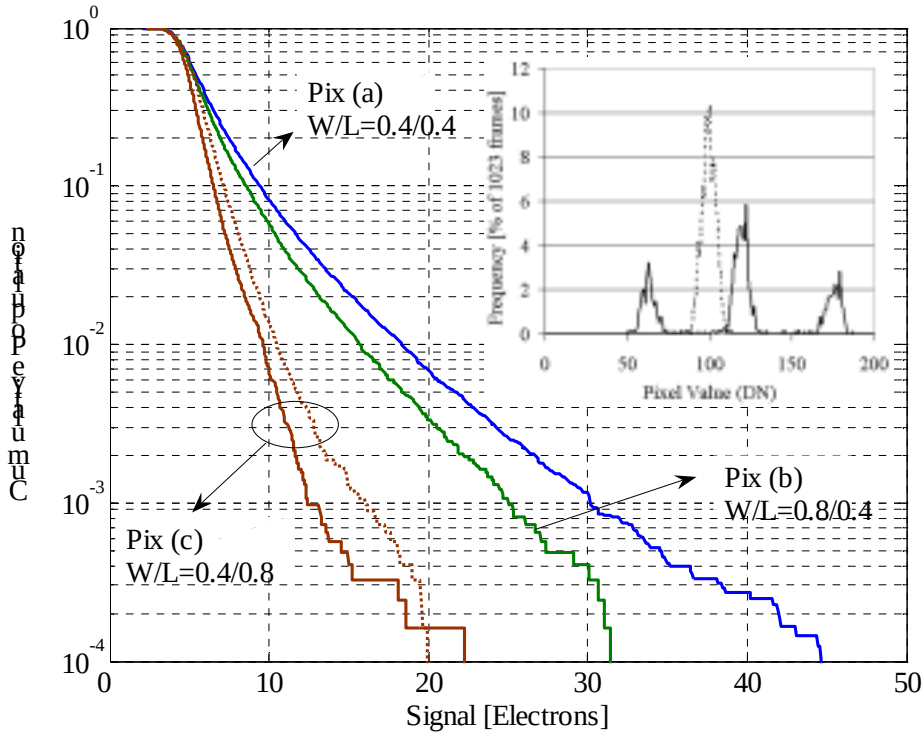

Figure 3 – Distribution of Pixel temporal noise within miniarray of 150x150 pixels for three different SF sizes; inner frame: Occurrence of pixel value (short integration time in dark) in 1023 consecutive frames for typical "quiet" (below 10^{-1} in the cumulative plot) and typical "noisy" pixel (above 10^{-3} in cumulative plot)