Integrated Processes for Detector Back Illumination*

Richard C. Westhoff†, Robert K. Reich, Andrew H. Loomis, James A. Gregory
MIT Lincoln Laboratory, 244 Wood Street, Lexington, MA USA 02420

Back-illuminated imagers can have high quantum efficiency at ultraviolet and x-ray wavelengths. Most back-illumination (BI) processes have limitations (e.g. fragility of thinned substrates[1], or the presence of epoxy[2], gold[3] or other bonding agents) that limit their applicability and process latitude. For example, these bonding agents limit BI processing at elevated temperature (i.e. ~400°C, hydrogen sintering), resulting in relatively high dark currents. More recently, 3D integration processes based on oxide bonding have addressed some of these issues for thin detector structures[4]. We describe BI processes, based on low-temperature oxide bonding, which can be integrated into the process flow of microelectronics fabs. The BI process faces two main challenges:

1. The need to produce thick (10-75 µm) active layers.
2. The need for high bond yield (~100%), due to the large detector area.

The first requirement makes it difficult for the gases that evolve at the bonded oxide-oxide interface to diffuse out of the structure without causing voids at the interface. This out-gassing occurs in low-temperature oxides (deposited thermally or plasma enhanced) at temperatures between ~275-400°C, and forms large voids at the bonded interface, as shown in Figure 1, which compares an image from a scanning acoustic microscope (SAM from Sonoscan™) to a thru-wafer IR image. The inspections are seen to be equivalent, but the SAM images provide more contrast and better sensitivity, particularly for small voids. The bonded region at the edge of the wafer (~40 mm), suggests that the interface gases could be "vented" by etching trenches in the oxide before bonding. Additionally, annealing the deposited oxide at a temperature above the final sintering temperature should reduce the out-gassing at the interface. The effect of a chemical mechanical planarization (CMP) step after the trench etching process was also investigated.

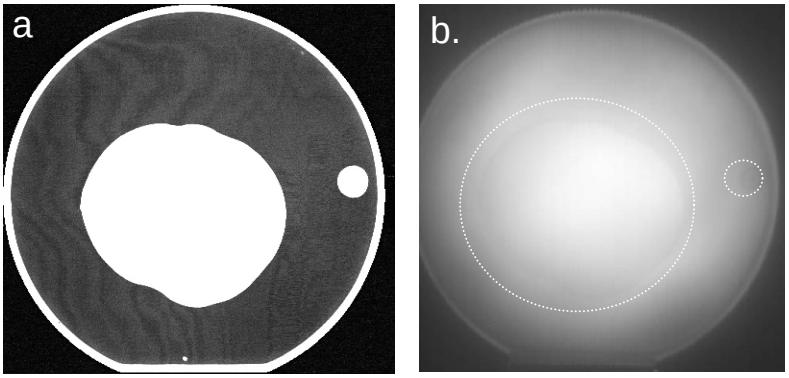

Figure 1. Scanning acoustic microscope (SAM) image (a) and IR transmission image (b) of plasma oxide-thermal oxide bonded wafer pair number 2/16 sintered at 400°C. Large void (white region) forms due to gas evolution at the bond interface during the sinter step.

The initial parameters and results of this experimental approach are summarized in Table I. Wafer pairs included a thermal oxide handle wafer and a device wafer with plasma enhanced chemical vapor deposition (CVD) oxide deposited from silane and oxygen. Since the plasma oxide as deposited is too rough (~6 nm RMS) for bonding purposes, the roughness is reduced to the 0.3-0.4 nm RMS level using CMP of the oxide, smooth enough to enable oxide-oxide bonding. Following CMP, the plasma oxide was annealed at 450°C in nitrogen for 30 minutes. The wafers were then patterned using photoresist and trenches 200 µm wide and 0.5µm deep were etched in the plasma oxide on the device wafers. In some cases a short follow-up, "kiss" CMP was done to remove possible defects caused by the patterning and trench etching.

The experimental results indicate that the absence of the trenches leads to large voids in the wafer center after post-bond sintering (Figure 2), even when the wafers are essentially void free just after bonding. Pre-bond annealing (Figure 3) also appeared to reduce the size of the voids. The effect of the clean and of the kiss CMP after trenching was less significant. On the initial three wafers the combination of trenches and nitrogen annealing before bonding

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† westhoff@ll.mit.edu, 781-981-3282 (voice), 781-981-3433 (fax)

produced bonds that survived sintering without forming large area voids. These bonded wafers also proved capable of withstanding the backgrinding and CMP process to ~60µm thickness without loss of the active layer.

Waf. No.	Device wafer	CMP	Pre-bond N2 Anneal	Trench	Kiss CMP	Clean	H2 Sinter	IR inspection results
2/16	No-pattern	Yes	450°C, 30 min	No	No	RCA-1, No megasonic	400°C, 60 min	5 cm dia. void ctr.
3/17	No-pattern	Yes	450°C, 30 min	No	No	H_2O_2, No megasonic	400°C, 60 min	2 cm dia. void ctr. & edge
5/18	Pattern	Yes	450°C, 30 min	Yes	Yes	RCA-1, No megasonic	400°C, 60 min	1 mm-size void
6/19	Pattern	Yes	450°C, 30 min	Yes	Yes	H_2O_2, No megasonic	400°C, 60 min	2 mm-size voids
10/20	Pattern	Yes	No anneal	Yes	Yes	H_2O_2, No megasonic	400°C, 60 min	5 cm dia. void ctr.
11/21	Pattern	Yes	450°C, 30 min	Yes	No	H_2O_2, No megasonic	400°C, 60 min	2 mm-size voids
12/22	Pattern	Yes	450°C, 30 min	No	Yes	H_2O_2, No megasonic	400°C, 60 min	5 cm dia. void ctr. & edge

Table I. Results of plasma oxide-thermal oxide bonding: effect of pre-bond anneal, trench, kiss-CMP and clean.

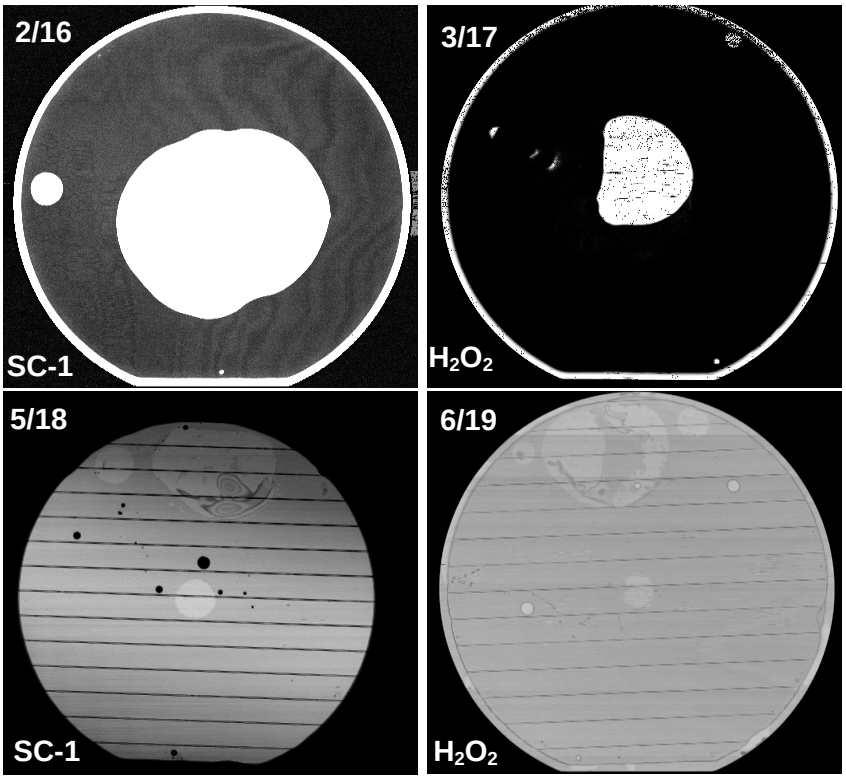


Figure 2. Comparison of SAM images of bonded wafer pairs 2/16 and 3/17 (non-trenched) versus wafer pairs 5/18 and 6/19 (trenched) with different pre-bond cleans. The device wafer from wafer pairs 2/16 and 3/16 have not been thinned while that of wafer pairs 5/18 and 6/19 have been thinned, causing the lighter wafer grey scale in the images. Lines in the image are the buried trenches that be confined in the streets between devices.

The smaller voids were determined (by microscope inspection using an infrared camera) to be caused by particles trapped at the interface. This is illustrated in Figure 4, which shows a void on a wafer, which is traced to a defect at the bond interface at the center of the void. Nearly all the small voids observed in the IR camera inspection were observed to have particles/defects at the center of the voids.

Because of the need to back-illuminate large imager devices, bonding yield is very important. For this reason, the pre-bond cleaning of the wafers was further studied to determine how to reduced particle-caused voids. This study compared RCA-1, RCA-1 & 2 cleans with megasonic energy, to RCA-1 and hydrogen-peroxide cleans without megasonic energy. The results indicated the use of RCA-1 clean followed by the use of megasonic energy were the

largest factors for reducing particulate-voids. RCA-1 only with megasonic energy produced the best results, and produced wafers that were free of small, particle related voids after sintering, as seen in Figure 5.

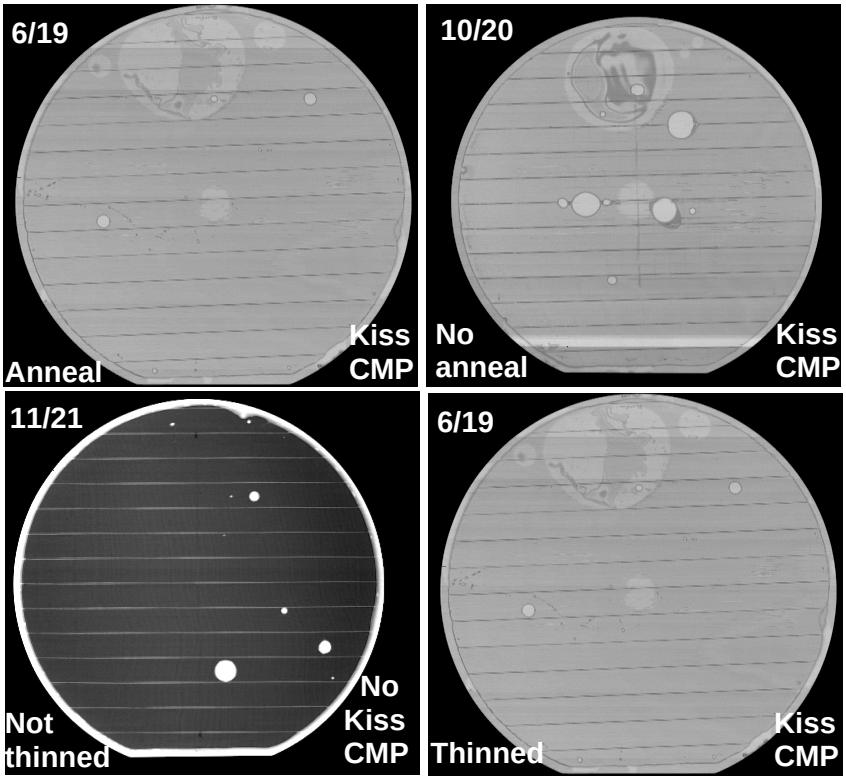


Figure 3: Comparison of SAM images of bonded wafer pairs that received a pre-bond anneal versus non-annealed wafer pairs and wafer pairs with and without a "kiss-CMP" after trenching. The device wafer of wafer pairs 6/19, 10/20 have been back thinned, while that of wafer pair 11/21 has not. Wafer pair 6/19 is shown twice for comparison of bonding with and without "kiss CMP" and with pre-bond anneal.

We have begun this BI process on device wafers with photodiode arrays. The dark current of the photodiodes was first measured in the front-illuminated condition. These device wafers have been oxide-oxide bonded (Figure 6), and back-side thinned to ~50 µm. They received back-side passivation (ion implant/t laser anneal process) followed by back-side bonding to a quartz wafer. The front-side handle wafer will next be removed, and contacts opened for testing. Following BI processing they will be used to test the effectiveness of sintering in reducing dark current in the devices.

We expect to demonstrate a BI process on photodiodes using oxide-oxide bonding shortly. It will first be used for back-illuminating avalanche photodiodes and later for CCD devices.

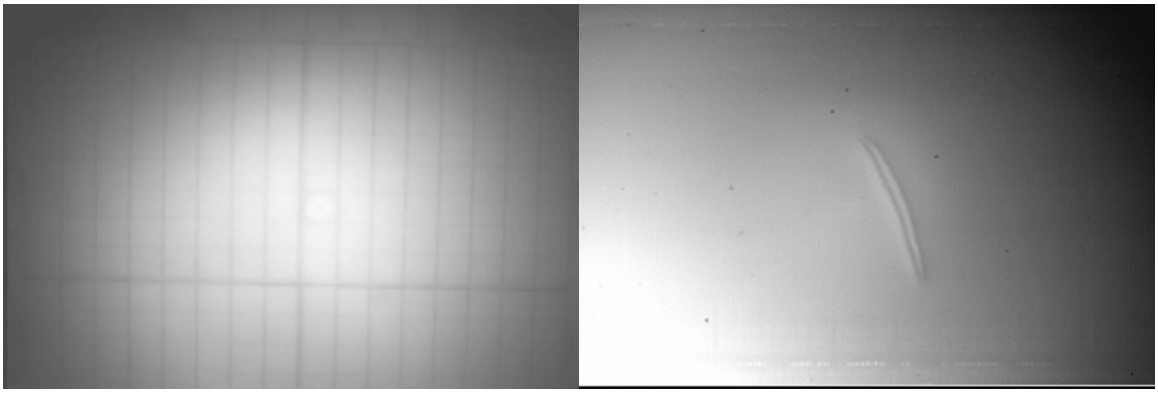


Figure 4. Result of through-wafer microscope inspection using an IR camera of voids to determine their cause. Left image is macroscopic IR image, while right is an IR micrograph of the void area.

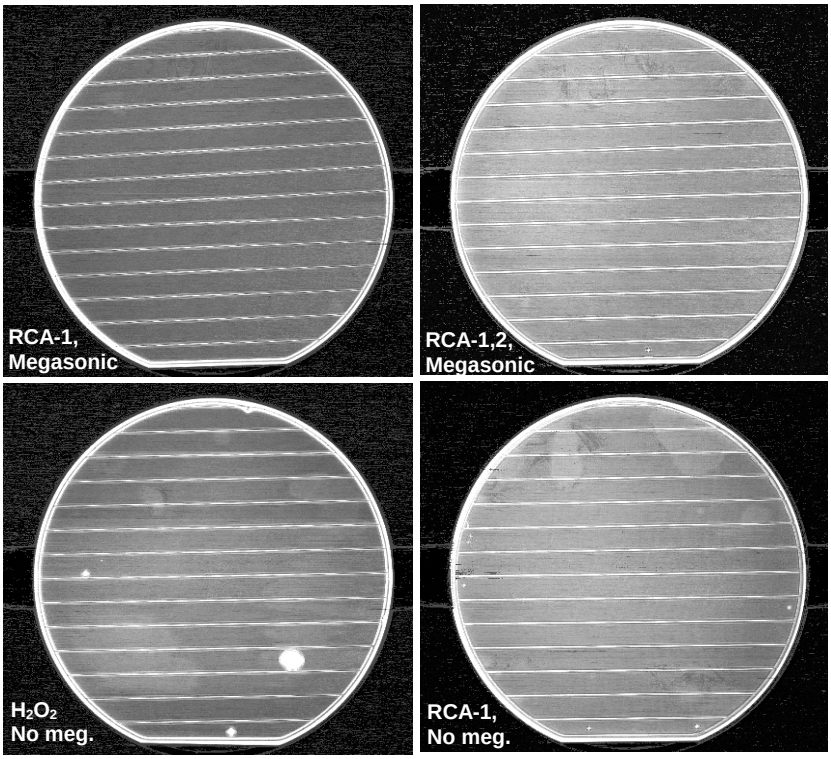
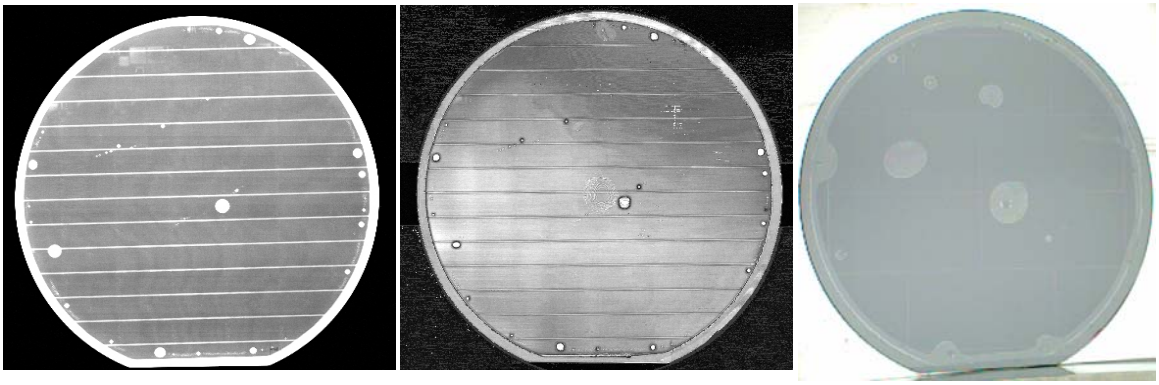


Figure 5. Sample of SAM images comparing various pre-bond cleans of plasma oxide bonded wafers after hydrogen sinter at 400°C. Wafer pairs with RCA-1 clean using megasonic energy are void free, while those using RCA-1 &2, hydrogen-peroxide or RCA-1 without megasonic energy have more voids. For the RCA-1 with megasonic energy, the edges are debonded, and the trenches are visible, but no other voids are observed.



Post bond – pre thin, pre sinter

Post thin, ion implant, laser anneal – post sinter

Post oxide – quartz bond

Figure 6. Scanning acoustic microscope images of a wafer with photodiode array devices bonded to a plasma oxide wafer. Voids are present due to the use of a non-optimized cleaning process, but no large voids are visible. Far right is an optical image of the photodiode wafer back-side after it was bonded to a quartz wafer.

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