Three-Dimensional Integration Technology for Advanced Focal Planes*

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Introduction

Over the last several years MIT Lincoln Laboratory (MIT-LL) has developed a three-dimensional (3D) circuit integration technology that exploits the advantages of silicon-on-insulator (SOI) technology to enable wafer-level stacking and micrometer-scale electrical interconnection of fully fabricated circuit wafers[1].

Advanced focal plane arrays have been the first applications to exploit the benefits of this 3D integration technology. The massively parallel information flow present in 2D imaging arrays maps very nicely into a 3D computational structure as information flows from circuit-tier to circuit-tier in the z-direction. To date, the MIT-LL 3D integration technology has been used to fabricate four different focal planes including: a 2-tier 64 x 64 imager with fully parallel per-pixel A/D conversion[2]; a 3-tier 640 x 480 imager consisting of an imaging tier, an A/D conversion tier, and a digital signal processing tier; a 2-tier 1024 x 1024 pixel, 4-side-abutable imaging module for tiling large mosaic focal planes[3]; and a 3-tier Geiger-mode avalanche photodiode (APD) 3-D LIDAR array, using a 30 volt APD tier, a 3.3 volt CMOS tier, and a 1.5 volt CMOS tier[4]. This last focal plane is an excellent example of one of the principal strengths of the 3D integration technology—the ability to integrate the best technology for the desired function within each tier of the circuit stack.

This talk will provide a brief overview of MIT-LL's 3D-integration process, and discuss some of the focal plane applications where the technology is being applied including a mixed material short-wave infrared (SWIR) focal plane array.

3D Technology

3D focal planes and circuits are fabricated by transferring and interconnecting fully fabricated 150-mm SOI substrates to a base wafer. The base wafer can be a high fill factor detector wafer or another circuit wafer and does not have to be a SOI substrate. The assembly process and a 3D chip consisting of three tiers are shown in Figure 1. Each functional section is labeled a tier, in a 3D system of n tiers, and consists of the interconnect and active devices. Tier 2 is transferred to the base tier, tier 1, after face-to-face infrared alignment, and oxide-oxide bonding at 150-275°C. The handle silicon of a transferred tier is removed by grinding the silicon to a thickness of ~50 µm followed by a silicon etch in a 10% TMAH solution at 90 °C. Since the ratio of silicon to BOX etch rates in TMAH is 1000:1, the handle silicon is removed without attacking the BOX and without introducing a thickness variation in the transferred tier, a factor that is essential when forming the vertical connections, or 3D vias. For this reason all circuits to be transferred are fabricated with SOI substrates. Then 3D vias are patterned and etched through the BOX and deposited oxides to expose metal contacts in both tiers. The fully depleted SOI (FDSOI) transistors are mesa isolated and the 3D vias are defined and etched through existing dielectric regions in the field, so that lining the vias with a deposited dielectric is not required to achieve insulation between the vertical connections. The 3D vias are then filled with damascene tungsten plugs planarized by chemical mechanical polishing (CMP) to electrically connect the two tiers. A third tier, tier 3, can then be added to the tier 1-2 assembly using the same processes, except that the front side of tier 3 is bonded to the BOX of tier 2, and 3D vias connect the top-level metal of tier 3 to the first-level metal of tier 2. The 3D chip is shown after bond pads are etched to expose the back of the first-level metal for probing and wire bonding. If the 3D chip is a digital circuit, the bond pads are etched through the BOX and deposited oxides of tier 3. If it is a back-side-illuminated imager, tier 1 is a detector wafer in which photodiodes were fabricated. An additional transfer to a carrier wafer is then required, and bond pads are etched after thinning the back side of the detector wafer to tune the detector layer to the required optical absorption. The cross-sectional scanning electron micrograph (SEM) of a three-tier ring oscillator shown in Figure 2 illustrates interconnections between tiers and the compactness possible with the 3D technology. Figure 3 shows some of the new technology developments including stacked 3D vias, and scaled 3D vias. In its current form the 3D integration technology can support ~1-µm-diameter 3D-vias on a 3.4 µm pitch. Of the three enabling technologies for 3D integration (precision wafer-to-wafer overlay, low temperature oxide bonding, and high-density 3D vias) it is the wafer-to-wafer overlay tolerance that has the largest impact on 3D via pitch. Figure 4 shows typical wafer-to-wafer overlay data for the precision alignment tool designed and fabricated at MIT-LL. This tool routinely provides a 0.5 µm (3σ) overlay tolerance on fully fabricated 150-mm-diameter wafer pairs.

Focal Plane Applications of 3D Technology

The 3D technology has been used to fabricate several different focal planes at MIT-LL. Figure 5 shows the image of a 4-side-abuttable, 1024x1024, 8µm-pixel pitch, 100% fill factor visible focal plane. This design enables the construction of large focal plane arrays with minimal (~3 pixel) seam loss.

Figure 6 shows and a 3-tier Geiger-mode avalanche photodiode (APD) 3-D LIDAR array, using a 30 volt APD tier, a 3.3 volt CMOS tier, and a 1.5 volt CMOS tier.

Figure 7 shows the application of the 3D integration technology to a 150-mm-diameter InP wafer. A SOI CMOS circuit layer was successfully transferred and interconnected with perfect yield to a metal landing pad on the compound semiconductor wafer. Building on this demonstration, MIT-LL is working on a 3D-integrated SWIR focal plane array using an InGaAs detector wafer.

Summary

A three-dimensional circuit integration technology based on silicon-on-insulator layer transfer and micron-scale 3D interconnects has been developed. The 3D technology allows two or more different process technologies to be stacked and interconnected enabling complex focal architectures with ideal fill-factors and a broad range of spectral sensitivities.

* *This work was sponsored by the Defense Advanced Research Projects Agency under U.S. Air Force contract FA8721-05-C-0002. Opinions, interpretations, conclusions, and recommendations are those of the authors and are not necessarily endorsed by the Department of Defense.*

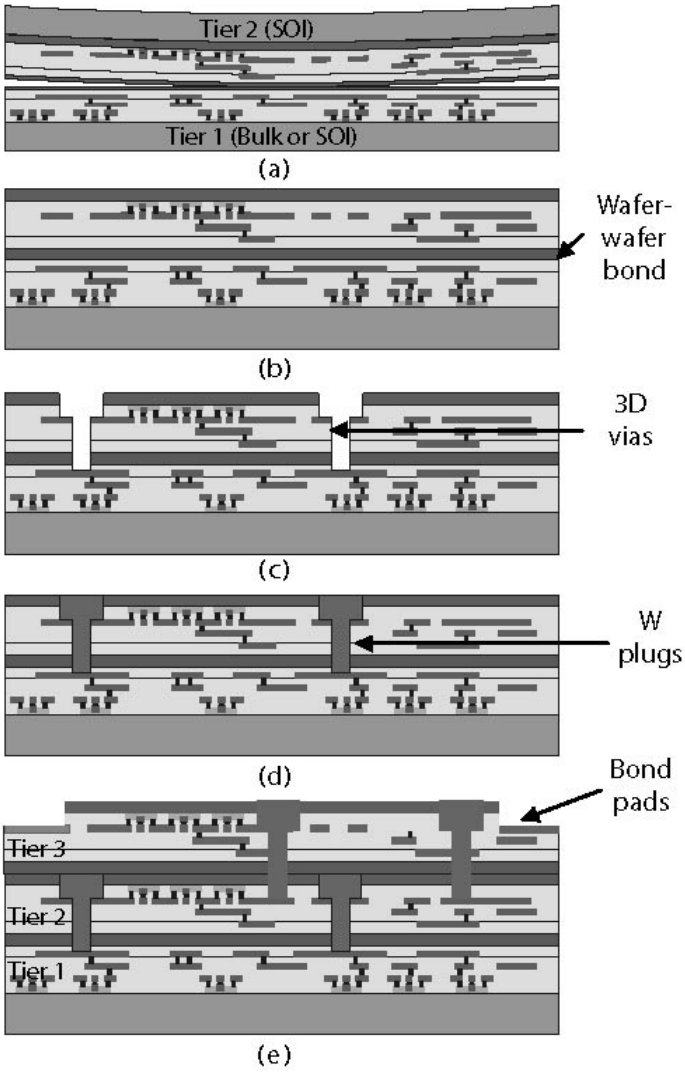

Figure 1. Assembly process for a 3D chip: (a) Two completed circuit wafers are planarized, aligned, and bonded face to face; (b) the handle silicon is removed; (c) 3D vias are etched through the deposited BOX and the field oxides; (d) tungsten plugs are formed to connect circuits in both tiers; and (e) after tier 3 is transferred, bond pads are etched through the BOX for testing and packaging.

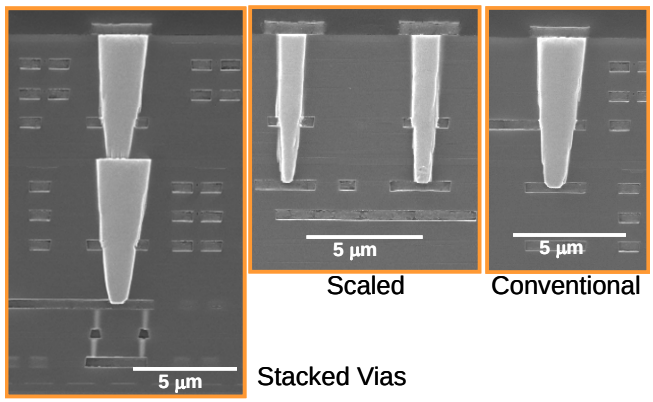

Figure 3. Cross-sectional SEM images of 3D-vias used in the 3D interconnect technology. On the left are stacked 3D-vias which can be used to provide a direct connection from the top-most tier to the bottom-most tier (tier-3 to tier-1 in this case). These metal plugs can also double as thermal vias to carry heat out of the 3D-stack for high performance circuit applications. The two images on the right show a conventional sized 3D-via next to the scaled via now being implemented in the MIT-LL technology. This via (~1-µm-diameter via) can support 3D-via pitches of 3.4 µm.

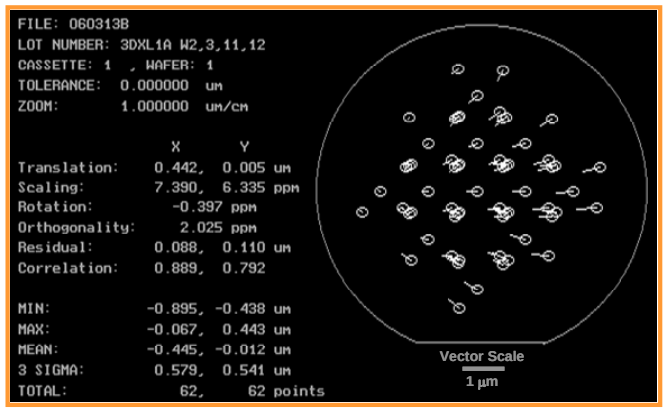

Figure 4. Wafer-to-wafer overlay tool measurement of two fully processed and 3D-inteconnected 150-mm-diameter circuit wafers. Typical overlay tolerances of 0.5 µm (3σ) are obtained with the MIT-LL precision aligner/bonder. Wafer-to-wafer overlay is the principal factor determining 3D-via pitch.

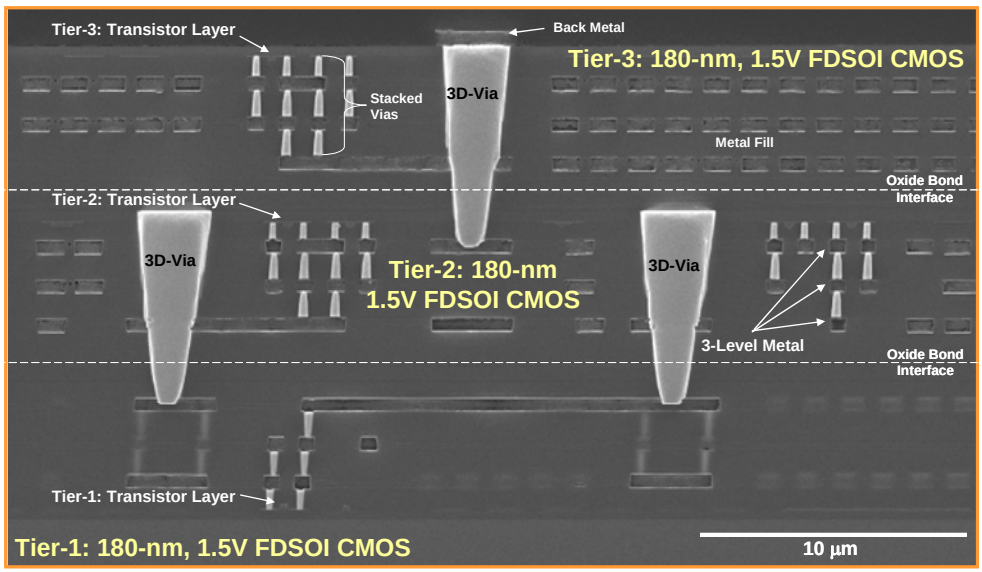

Figure 2. Cross-sectional SEM of a functional three-tier ring oscillator circuit designed to test all three active transistor tiers and all ten metal interconnect layers. The tiers are bonded and interconnected with tungsten plug 3D-vias; the conventional interlevel connections are seen in in each of the 3 FDSOI tiers. Note that the 3D vias are located in the isolation (field) region between transistors.

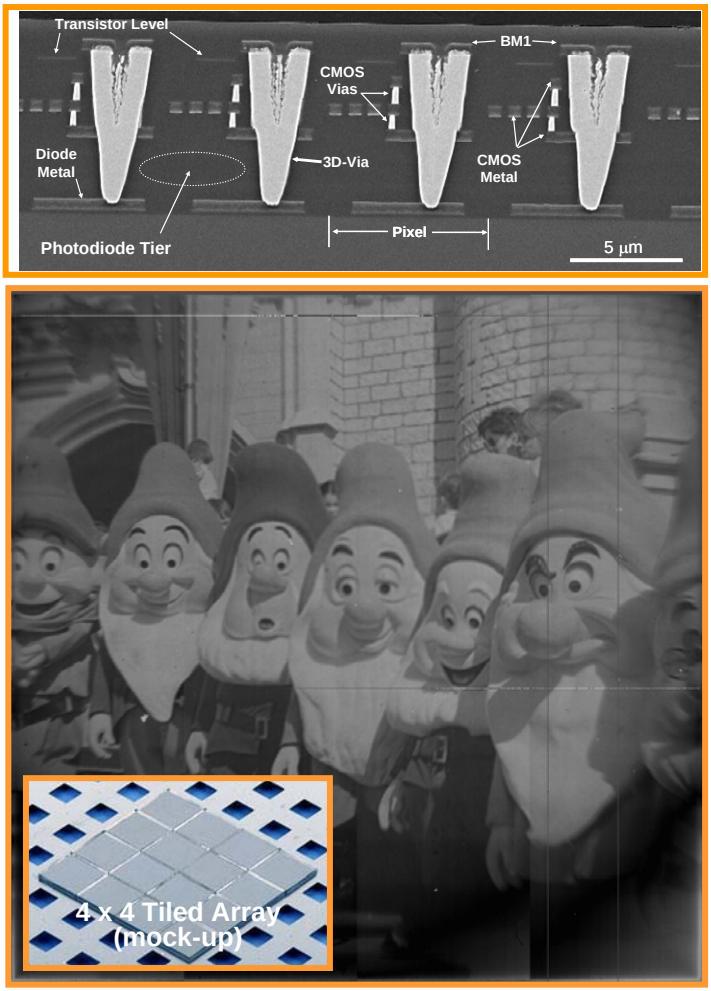

Figure 5. Top image is a cross-sectional SEM of four pixels of a two-tier, 4-side-abuttable, 1024x1024, 8µm-pixel pitch, 100% fill factor visible focal plane. Below is an actual 1024x1024 test image from the 3D integrated focal plane. Inset image is a mock-up 4x4 imager tile "mosaic" array, showing how the 4-side-abuttability enabled by the 3D integration can allow larger focal planes to be tiled together with minimal seam loss (~3 pixels).

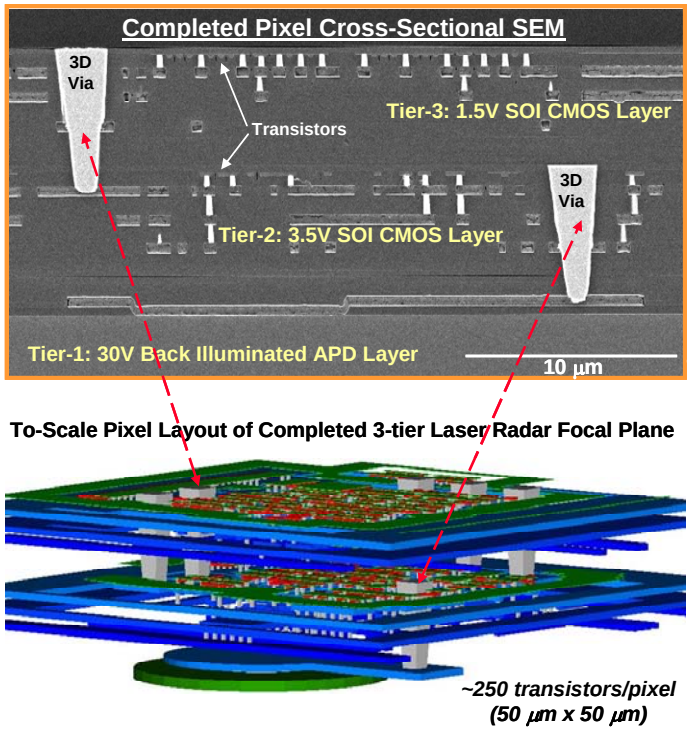

Figure 6. Cross-sectional SEM of a single pixel from a functional 3-tier Geiger-mode avalanche photodiode (APD) 3-D LIDAR array. Tier-1 is a 30 volt APD tier which is 3D-integrated to tier-2, a 3.3 volt CMOS interface circuit tier, which is 3D-integrated to tier-3, a 1.5 volt CMOS high-speed timing circuit tier. Below the cross-sectional image is a CAD drawing of the completed pixel layout. There are ~250 transistors and six 3D-vias per pixel in this circuit.

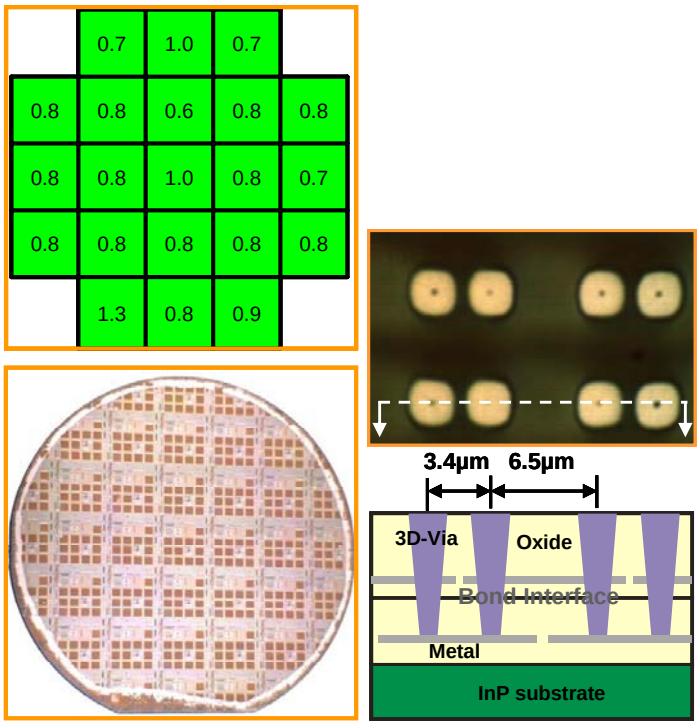

Figure 7. Bottom left is a photograph of a SOI CMOS circuit tier 3D-integrated to a pattern 150-mm-diameter InP wafer. This two-tier stack was used to evaluate the effectiveness of the 3D integration process with mixed semiconductor material systems. Top left is a die yield map showing 100% yield of 10,000-link 3D-via-chains. The number in each green box is the average resistance per 3D-via-link in the chain. Right side of figure is top-down image and cross-sectional drawing of a section of the completed 3D-via-chain.

References

[1]J.A. Burns, et. al., "A Wafer-Scale 3-D Circuit Integration Technology," *IEEE Transactions on Electron Devices,* vol. 53, no. 10, pp. 2507-2516, Oct. 2006.

[2]J.A. Burns, et. al., "Three-dimensional integrated circuits for low power, high bandwidth systems on a chip," *2001 ISSCC Int. Solid-State Circuits Proceedings, Digest of Technical Papers* vol. 44, pp. 268-269, Feb. 2001.

[3]V. Suntharalingam, et. al., "Megapixel CMOS Image Sensor Fabricated in Three-Dimensional Integrated Circuit Technology," *2005 ISSCC Int. Solid-State Circuits Proceedings, Digest of Technical Papers* vol. 48, pp. 356-357, Feb. 2005.

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