Pixel-level A/D conversion: comparison of two charge packets counting techniques

A. Peizerat, M. Arques, P. Villard, J-L. Martin
CEA/LETI - MINATEC
Grenoble, France
arnaud.peizerat@cea.fr

***Abstract*— A comparison between two techniques for pixel-level ADC in CMOS image sensors is presented. As the charge represents accurately the amount of illumination, the principle of both techniques consists in counting small charge packets which come from the detector. Based on a 0.13 µm CMOS technology, simulation results and first measurements are presented showing that the LSB value can be reduced to 1900 electrons with a static power of 250nW per pixel. For the moment, due to the technology available, this technique is restricted to medium size pixels, i.e. 50x50 µm^2 or 25x25 µm^2 when the fill factor is close to 100%.**

I. INTRODUCTION

Pixels of an image sensor are composed of two parts: the detector, which converts incident photons energy into electron-hole pairs, and the readout electronics, which converts these electron-hole pairs into a readable signal. In the conventional Active Pixel Sensor (APS), this signal is an analog voltage drop which is transferred off-chip, since the detector current discharges the integration capacitor (C_{INT}). Because reliability and performance are always an issue, and also because of the evolution of technology, the Analog-to-Digital Conversion (ADC) tends to be integrated into the CMOS image sensor. The purpose of a pixel-level conversion, in comparison to chip or column-level ADC, is first, power reduction, thanks to a lower conversion frequency, and second, noise reduction, because analog multiplexing is suppressed [1]. The main constraint is, in fact, the limited pixel area.

Several papers suggest different methods for pixel-level ADC. A 1st order ΔΣ approach with multiplexed pixels [2] shows a 7-bit resolution but requires off-chip decimation filtering. The MultiChannel bit-Serial (MCBS) technique [3], which associates the single-slope ADC concept with the Gray-code quantization, is very efficient for small pixels, but the resolution obtained is of 8 bits only. With separate MSB and LSB conversions [4], a 12-bit resolution is reached but linearity is affected. An ASIC for medical applications [5] presents good performance but the LSB value of the ADC is too large because of the application specifications. Inspired by those papers, we present here a comparison between two techniques, which we call "voltage reset technique" and "charge reset technique". In both techniques, a pixel-level ADC is performed with a low LSB value, good linearity, and high resolution.

II. FIRST APPROACH OF THE TWO TECHNIQUES

The common principle which consists in counting charge packets coming from the detector is also called charge-balancing technique [6]. As illustrated in Fig. 1, I_{DET}, created by the illumination, discharges C_{INT} until V_{INT} crosses V_{TH}, then the comparator commands the injection of Q_0 at the integration node and the counter (not drawn on the figure) is incremented by one. At the end of integration time, the counter contains the number N. Since the LSB value of the A/D conversion is Q_0, N.Q_0 has been detected. The only difference between the two techniques is the way Q_0 is generated. In the "voltage reset" case, Q_0=C_{INT}.ΔV and so the LSB is highly dependent on V_{TH}. This technique is thus very sensitive to the performance of the comparator but allows an efficient layout. In the "charge reset" case, Q_0 is generated by a charge injector, thus it relaxes constraints on the comparator and on C_{INT} precision, providing the charge injector has good performance.

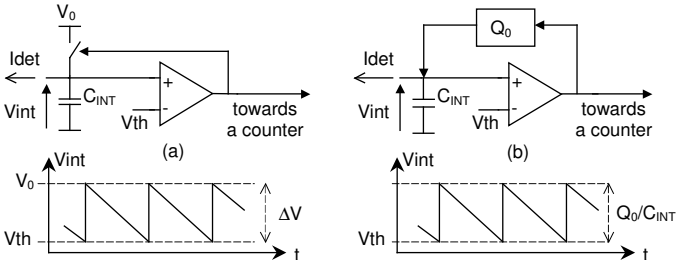


Figure 1. principles of the two techniques (a) voltage reset technique and (b) charge reset technique, assuming I_{DET} is constant

For these two techniques, you can trade off the number of bits against the conversion time which depends on the frame rate. In other words, with twice the integration time and one more flip-flop in the counter, the dynamic range is doubled. That's the reason why it is particularly appropriate to discuss the LSB value, Q_0 , which is not dependent on the conversion time. Indeed the performance of the conversion is given by the properties of Q_0.

III. VOLTAGE RESET TECHNIQUE DESIGN

Since $Q_0=C_{INT}.\Delta V$, this technique is sensitive to C_{INT} and ΔV variations. ΔV variations can be due to threshold voltage variations (V_{TH}) or reference voltage variations (V_0).

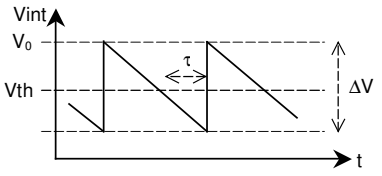


Figure 2. Influence of the delay (τ) of the comparator when $I_{DET}>Q_0/\tau$

Considering the comparator as a first order lowpass filter with a time constant τ, the effective threshold seen by V_{INT}, Fig. 2, is given by:

$$V_{TH\_eff} = V_0\text{-}V_{TH} + \tau.I_{DET}/C_{INT} \quad (1)$$

As a result, Q_0 varies depending on the value of I_{DET}, the linearity error of the A/D conversion is then:

$$\frac{\Delta Q_0}{Q} = \frac{\tau \cdot I_{DET}/C_{INT}}{V_0 - V_{TH}} \quad (2)$$

Considering the input referred noise e_n of the comparator and the thermal noise introduced by the reset switch, Q_0 varies at each reset. So, assuming that the reset noises are not correlated with one another, the standard deviation $\sigma_{READOUT\_e-}$ (in electrons), at the end of integration time can be written as:

$$\sigma_{READOUT\_e-} = \frac{1}{q} \cdot \sqrt{N \cdot C_{INT}^2 e_n^{\,2} + N \cdot kTC_{INT}} \quad (3)$$

where q is the charge of a single electron, k the Boltzman's constant and T the temperature.

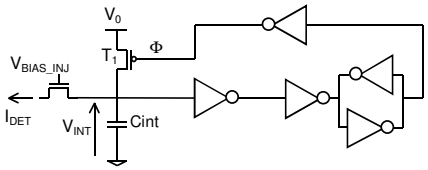


Figure 3. Schematic of a pixel

In our design, Fig. 3, we chose the smallest value for C_{INT} in order to minimize $\sigma_{READOUT\_e-}$. For that purpose, a common gate (or direct injection) transistor, T_{INJ}, is used in saturation or weak inversion region to make sure C_{INT} is not dependent on C_{DET}, the capacitance of the detector. This means that C_{INT} can be as small as possible, i.e., a parasitic capacitor. Of course, this implies that an I_{DET} -dependent pole is introduced. Suppose T_{INJ} in weak inversion, then the value of that pole is:

$$p = \frac{q}{n.k.T} \cdot \frac{I_{DET}}{C_{DET}} \quad (4)$$

where n is the ideality factor (≈1.2 for the process we use). That restriction has to be taken into account if the conversion time specification is very severe.

Fig. 3, the comparator is composed of a simple CMOS inverter and a trigger circuit. The CMOS inverter exhibits a good trade-off between bandwidth and power consumption. The trigger circuit introduces hysteresis and high gain to ensure noise immunity during the decision step and to prevent metastability.

IV. CHARGE RESET TECHNIQUE DESIGN

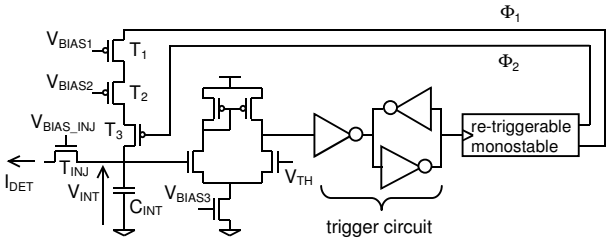


Figure 4. Schematic of a pixel

Fig. 4, the scheme of this technique is very similar to that of the voltage reset technique. Since Q_0 is not dependent on V_{TH} variations, the use of a differential pair with poor bandwidth but without big current spikes is possible. The trigger has the same function as previously.

When the output of the trigger circuit falls, a monostable circuit creates two pulses, Φ1 and Φ2, which control the charge injector (T1, T2 and T3) whose scheme is borrowed from CCD technology. Fig. 5, while Φ2 is high, Φ1 first fills the potential well formed by T1 and T2 with charges (Φ1 = '1') and then the charges are spilled out of the potentiel well (Φ1 = '0'). A certain amount of charges, Q_0, is thus stored under the gate of T2. Assuming that overlap and junction capacitors are negligible:

$$Q_0=C_{OX}.W_{T2}.L_{T2}.(V_{BIAS1}\text{-}V_{BIAS2})=C_{INJ}.(V_{BIAS1}\text{-}V_{BIAS2}) \quad (5)$$

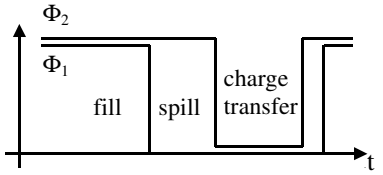


Figure 5. Timing diagram of Φ1 and Φ2

Then, when Φ2 falls, this amount of charges Q_0 is transferred onto the capacitor of the integration node. Fig 6 illustrates, thanks to a potential well representation, the different charge flows.

Both signals, Φ1 and Φ2, can be chosen to control the counter.

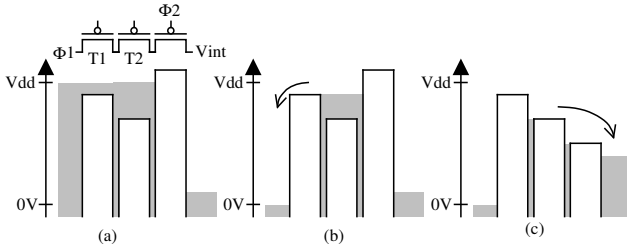


Figure 6. The different charge flows (a) the fill step, (b) the spill step and (c) the charge transfer step

For a given C_{INT}, the smaller Q_0 is, the lower the ΔV (= Q_0 / C_{INT}) will be each time the charge reset appears on the integration node, the worst option being that the comparator might not return to its waiting state because of the delay of the comparator (Fig. 7). The condition of this worst option can be expressed as:

$$I_{DET} > Q_0 / \tau \quad (6)$$

where τ is the delay of the comparator.

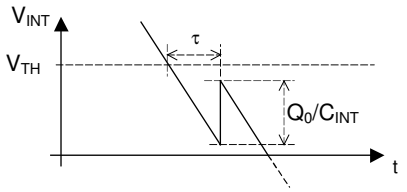


Figure 7. Influence of the delay (τ) of the comparator when $I_{DET}>Q_0/\tau$

This problem can be solved by the use of a retriggerable monostable circuit. If the comparator does not switch back after a charge injection, the circuit automatically re-triggers after a period τ_{MONO} lower than τ, the delay of the comparator. As shown in Fig. 8, it guarantees a good functionality until saturation when I_{DET} reaches the limit:

$$I_{DET} > Q_0 / \tau_{MONO} \quad (7)$$

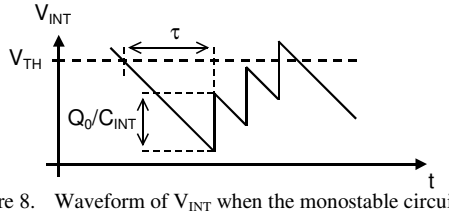


Figure 8. Waveform of V_{INT} when the monostable circuit re-triggers

For the calculation of noise, let's consider, as in the previous section, that the reset noises are not correlated with one another, then the standard deviation $\sigma_{READOUT\_e-}$, at the end of integration time can be written as :

$$\sigma_{READOUT\_e-} = \frac{1}{q} \cdot \sqrt{C_{INT}^2 e_n^{\,2} + N \cdot kTC_{INJ}} \quad (8)$$

where N is the number of charge resets and C_{INJ} is defined in (5). Compared to (3), the influence of e_n is negligible (except for great value of C_{INT}) because it does not increase with N. One can also note that the reset noise is not dependent on C_{INT} but on C_{INJ}, the capacitance of the charge injector.

V. Simulation Results

The results concern one pixel of each technique without the counter. The circuit was designed using a 0.13 µm process with 1.2 V power supply voltage. Integration time was set to 2 ms and the maximum I_{DET} to 5 nA (I_{DET_MAX}). So the maximum detected charge is 10 pC (Q_{MAX}). Given that the LSB value is 2000 electrons or 0.35 fC (Q_0), the resolution reached is slightly lower than 15 bits. The overall characteristics are summarized in Table 1.

Note that the noise results are expressed as the ratio of $\sigma_{DETECTOR\_e-}$ by $\sigma_{READOUT-e-}$. Indeed $\sigma_{READOUT\_e-}$ has to be compared to the RMS detector noise present at the input of the converter. Assuming that the detector is a photodiode, the noise is a conventional shot noise, and its standard deviation ($\sigma_{DETECTOR\_e-}$), in electrons, is :

$$\sigma_{DETECTOR\_e-} = \sqrt{I_{DET}\, T_{INT} / q} \quad (9)$$

In the case of a detector with a quantum efficiency, η, above one (e.g. detection of high energy photons), its standard deviation ($\sigma_{DETECTOR\_e-}$), in electrons, becomes:

$$\sigma_{DETECTOR\_e-} = \sqrt{\eta \cdot I_{DET}\, T_{INT} / q} \quad (10)$$

The ratio $\sigma_{DETECTOR\_e-}/\sigma_{READOUT\_e-}$ is then improved by $\sqrt{\eta}$.

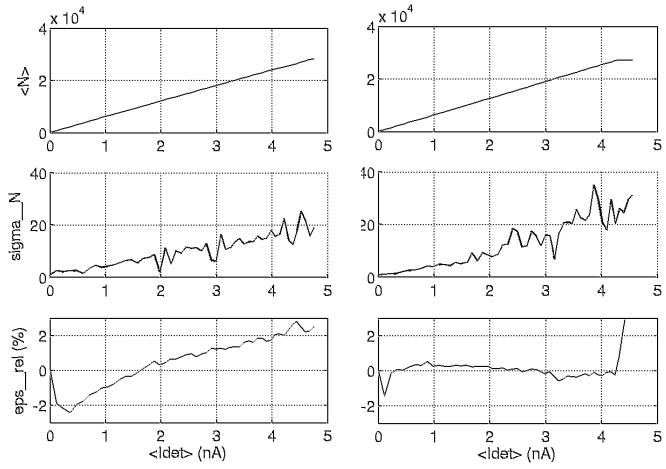
TABLE I. Summary of simulation results for 2 ms integration time

	Voltage reset	**Charge reset**
Idet range	[5 pA; 5 nA]	[5 pA; 5 nA]
LSB (electrons)	2000	2000
Linearity (over Idet range)	2%	0.2%
Noise ($\sigma_{DETECTOR\_e-}/\sigma_{READOUT\_e-}$)	3.4 @ 5nA	1.7 @ 5nA
Layout (w/o the counter)	8µm x 6µm	22µm x 12µm
Power (µW)	0.2 @ 5pA 1.4 @ 5nA	0.2 @ 5pA 1.5@ 5nA

VI. Experimental Results

A test-circuit was fabricated in a 0.13 µm process with 1.2V power supply voltage. As the objective was more to validate these pixel-level ADC techniques rather than to

realize an image sensor, this test chip only contains a few pixels. Each pixel is composed of the structure in Fig. 3 or Fig. 4, plus buffers and a photodiode acting as a low noise current source. The test consists then in lightening the chip with a LED and counting the generated pulses by software methods. For a given LED current, several acquisitions are carried out so as to extract the mean (<N>), the standard deviation (sigma_N) and the linearity (eps_rel) of the number of counted pulses. The curves of Fig. 9 give the evolutions of these features with the current I_{DET} measured by an on-chip reference-pixel.



(a) (b)

Figure 9. Mean, standard deviation and linearity error of N as a function of I_{DET} (a) for the voltage reset technique and (b) for the charge reset technique. N is the number of charge injections during 2 ms

TABLE II. SUMMARY OF EXPERIMENTAL RESULTS FOR 2 MS INTEGRATION TIME

	Voltage reset	**Charge reset**
Idet range	[5 pA; 4 nA]	[5 pA; 4 nA]
LSB (electrons)	1900	1900
Linearity (over Idet range)	4%	0.4%
Noise ($\sigma_{DETECTOR\_e}/\sigma_{READOUT\_e}$)	0.3 @ 4nA	0.1 @ 4nA
Power (µW)	0.25 @ 4pA 1.8 @ 4nA	0.25 @ 4pA 1.9@ 4nA

Experimental results are close to simulation results except for noise performance. Indeed noise is one order of magnitude larger than expected. Fig. 10 illustrates an experiment which consists, for the "charge reset" technique, in observing N (the number of counted pulses during Tint) over a large period of time. The presence of steps is an unexpected phenomenon. Those steps occur for the two techniques and their magnitude strongly depends on the chip being tested. The "worst" chips in our batch of 25 can show a ratio of 1% between the magnitude of the steps (ΔN) and the absolute value (N). Those technological fluctuations and a ΔN/N of 1% indicate that this phenomenon could be due to RTS (Random Telegraph Signal) noise. We are currently working on design solutions even if electrical simulators do not include RTS noise for the moment.

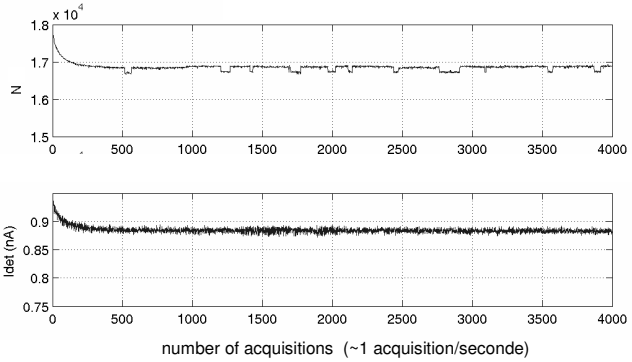


Figure 10. Measured results and apparition of steps when observing N (here for the charge reset technique) over a large period of time. T_{INT}=2ms, one acquisition lasts one second.

VII. CONCLUSION AND FURTHER RESEARCH

Two pixel-level ADC techniques have been developed achieving a 15-bit resolution over a 2 ms integration time, with good linearity and a very small LSB. The voltage reset version has a more efficient layout implementation and the charge reset version shows high linearity. For the moment, due to the technology available, these techniques are restricted to medium size pixels, i.e. 50x50 µm2 or 25x25 µm2 when the fill factor is close to 100%.

Noise reduction and dynamic range (DR) enhancement are subjects for further research. A 120 dB DR is expected at the cost of a reduced fill-factor.

REFERENCES

[1] B. Pain and E. R. Fossum, "Approaches and analysis for on-focal-plane analog-to-digital conversion," SPIE, vol. 2226, 1994, pp. 208-218.

[2] D. Yang, A.E. Gamal and B. Fowler, "A 128x128 pixel cmos area image sensor with multiplexed pixel-level A/D conversion," IEEE, Custom IC Conference, 1996, pp 303-306.

[3] D. Yang, A.E. Gamal and B. Fowler, "A nyquist-rate pixel-level ADC for CMOS image sensor," IEEE, JSSC, 1999, pp 348-356.

[4] J. RHEE and Y. JOO,. "Wide dynamic range CMOS image sensor with pixel level ADC," IEE, Electronics Letters, Vol. 39, No. 4, Feb. 2003, pp. 360-361.

[5] G. Mazza, R. Cirio, M. Donetti, A. La Rosa, A. Luparia, F. Marchetto and C. Peroni, "A 64-channel wide range charge measurement asic for strip and pixel ionisation detectors," IEEE, Transactions on Nuclear Science, Vol. 52, No. 4, Aug. 2005, pp. 847-853.

[6] P. Horowitz and W. Hill, The Art of Electronics, 2nd edition, Cambridge University Press, 1980, pp. 626-629.

[7] G. Grandbois and T. Pickerell, "Quantized feedback takes its place in analog-to-digital conversion," Electronics, October 1977.