

# Back-Illuminated, Three-Dimensionally Integrated CMOS Imager with In-Pixel CDS

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**Abstract:** We present a three-dimensionally (3D) integrated CMOS photodiode imager pixel array that includes pixel-level correlated double sampling to suppress reset noise. This 256 x 256 active pixel image sensor employs a FDSOI CMOS-based readout tier vertically interconnected to silicon photodiode pixels. A wafer-scale back-illumination process is used to achieve 100% fill factor photodiodes. Device testing is underway with simulations projecting an input referred noise target of 5 electrons.

## Introduction

Lincoln Laboratory has developed a wafer-scale process technology that enables the dense vertical interconnection of multiple circuit layers [1]. For image sensor applications the first circuit layer or tier is a silicon or compound semiconductor device and the second and subsequent tiers contain silicon-on-insulator (SOI)-based electronics. As shown in Figure 1, the circuit tiers are vertically interconnected through an oxide-bonded interface, and the detector tier may be thinned for 100% fill factor, back-illuminated operation. For mechanical support, an optional transparent substrate may be present, and openings may be included in the substrate for soft X-ray penetration. The combination of small wafer-to-wafer alignment tolerance (+/- 0.25  $\mu\text{m}$ ) and small 3D via size (1-2  $\mu\text{m}$ ) permits aggressively small pixels. Earlier we demonstrated a 1k x 1k CMOS visible imager [2] with 8- $\mu\text{m}$  x 8- $\mu\text{m}$  pixels, having a vertical interconnection at each pixel between photodiode and readout transistors. Fig. 2 shows a cross-sectional SEM through two pixels of this functional active pixel imager.

With dense vertical integration of pixel detector to associated transistors comes the significant benefit that greater area in the pixel footprint can be devoted to readout circuitry than could be accomplished in a conventional monolithic architecture. In this work we employ a simple noise suppression circuit to reduce reset noise, which can be the dominant noise source under low illumination.

## Pixel Design and Operation

To implement in-pixel reset noise substraction, we adapted a per-pixel “clamp” CDS circuit [3] to our 3-D SOI CMOS technology. Fig. 3 and 4 show the pixel structure and the timing diagram, respectively. The pixel consists of two reset switches (MRST1 and MRST2), two source followers (MSF1 and MSF2), a CDS capacitor (C2), and row selection transistors (M\_ROW and M\_ROWBAR). Reset noise reduction is accomplished by transferring the large  $kT/C_{pd}$  reset noise from the MRST1 reset to the much larger coupling capacitance C2.

The pixel is operated with a two-stage reset. In the first phase both MRST1 and MRST2 are held low (for p-MOS

reset transistors). Integration begins when MRST1 is raised. The noise from MRST1 is transferred to C2, where it is subtracted by the capacitor. Since the initial reset noise is subtracted, the operation is a form of correlated double sampling, here occurring internal to the pixel. Finally MRST2 is raised, causing a smaller  $kT/C2$  noise voltage to be sampled onto the capacitor.

Pixel layout for Tier-2 and Tier-1 are shown in Fig. 5 and 6, respectively. We use p-MOS reset transistors to allow complete reset of the photo-diode node, thus avoiding image lag. SOI transistor layout was driven to minimize parasitic leakage mechanisms; thus H-gate geometries and body-ties were employed where possible. A generous 24- $\mu\text{m}$  square was allotted to the pixel so that we could achieve a large in-pixel coupling capacitance (780fF). Much finer pixel sizes could be realized by using conventional (non-H-gate) transistor gate geometries, smaller coupling capacitance, or by elevating the coupling capacitance to an even higher third circuit tier.

## Fabrication Technology

Photodiodes and CMOS pixel electronics were fabricated in two separate 150-mm circuit wafer lots and assembled into a 3-D stack. The photodiode tier (Tier-1) consisted of p+n diodes in high-resistivity (>3000  $\Omega\text{-cm}$ , n-type) float-zone silicon substrates. The diode’s lateral doping profile is graded using implant masking and thermal annealing to minimize the surface contribution to dark current. The second tier (Tier-2) is fabricated using our 0.35- $\mu\text{m}$  FDSOI-CMOS process with 7.2-nm gate oxide, cobalt-silicide, and planar three-level-metal interconnect. After 3-D circuit stacking [1,2], the imager is prepared for illumination from the photodiode side; the detector tier silicon is thinned to approximately 50 $\mu\text{m}$ , coated with an antireflection layer, and then mounted onto a transparent support in a process sequence similar to that used to make back-illuminated CCDs [4]. Standard semiconductor equipment was used for all processing steps. An in-process view of the pixel transistors is shown in Fig. 7.

## Results

Fig. 8 shows a photograph of the completed chip after processing for back illuminated operation. This test array is 256x256 pixels, each 24- $\mu\text{m}$  square, with a chip footprint of roughly 6mm x 6mm. Initial testing confirms photoresponse from the array. Fig. 9 compares SPICE-based noise simulations to hand calculations for pixels with varying C2. SPICE predicts a noise target of 5-electrons rms, further dependent on other sources in the signal chain. We intend to present detailed test characterization results in June.

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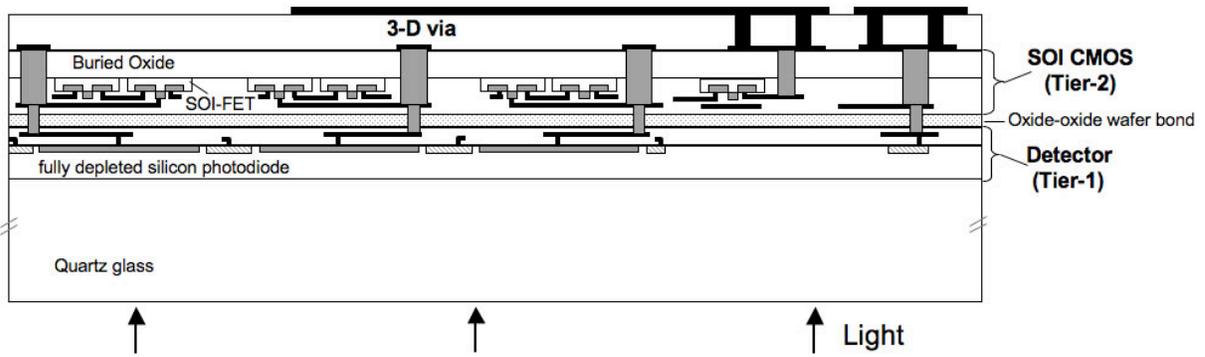


Fig. 1. Schematic diagram of 3-D stacked image sensor circuit. Tier-1 is a silicon photodetector wafer and Tier-2 is an inverted SOI-CMOS wafer.

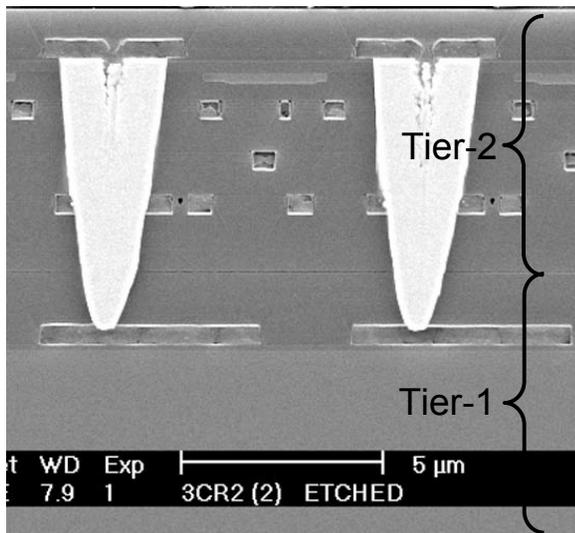


Fig. 2. Cross sectional SEM micrograph through 8- $\mu\text{m}$  pixel, 3-D integrated CMOS image sensor [2]. The oxide-oxide bond between the two tiers has been decoratively etched to highlight its position.

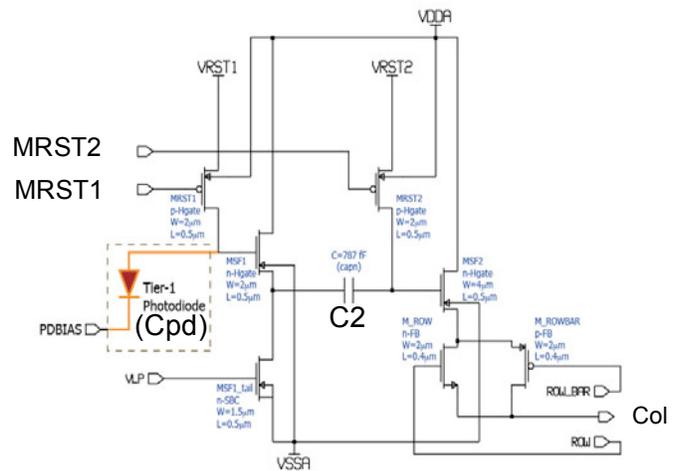


Fig. 3. Three-dimensionally integrated pixel schematic.

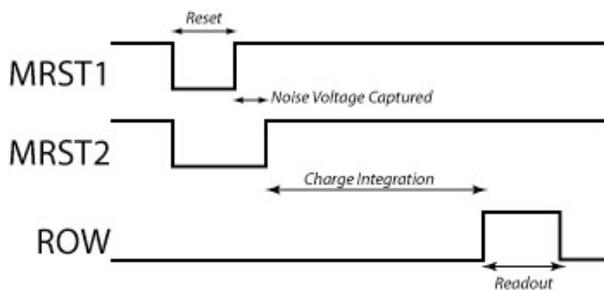


Fig. 4. Pixel timing diagram to implement reset noise reduction. (Based on [3])

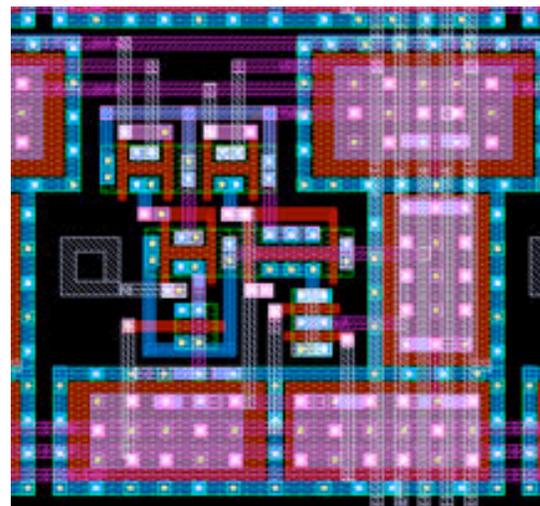


Fig. 5. Pixel Layout in Tier-2 which includes reset gates, CDS capacitor, and readout transistors. (24 $\mu\text{m}$  square)

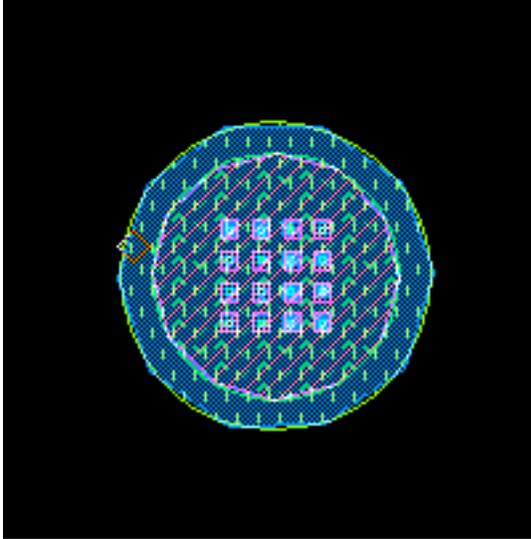


Fig. 6. Photodiode pixel layout in Tier-1 (24µm square).

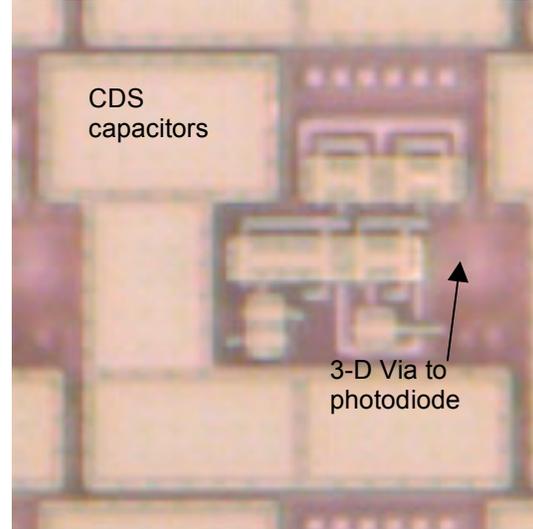


Fig. 7. In-process photomicrograph of pixel after 3-D layer transfer. The SOI-CMOS transistors are seen to be inverted, with active silicon islands now above the polysilicon gates.

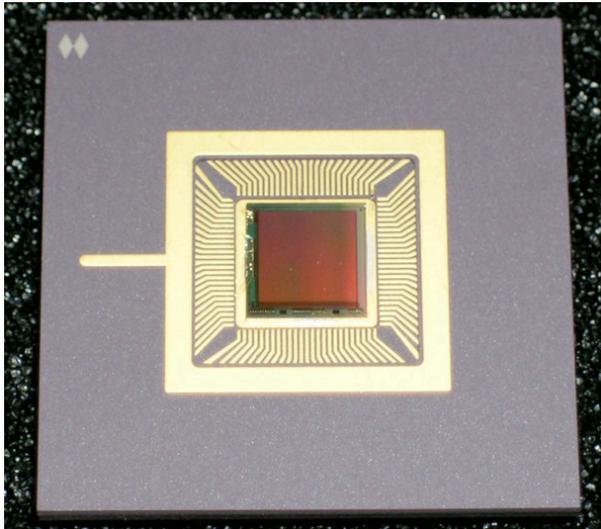


Fig. 8. Completed 256x256 pixel array after processing for back-illuminated operation.

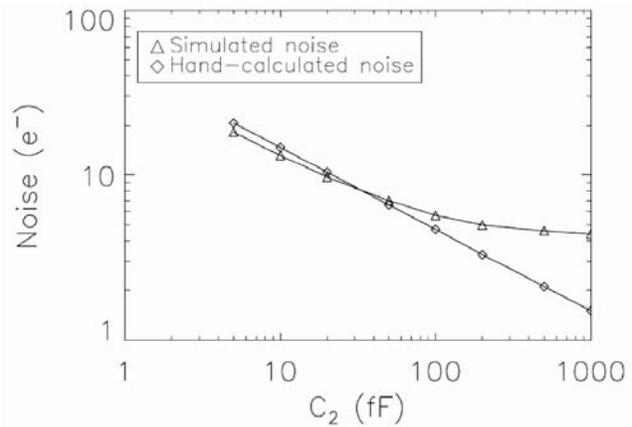


Fig. 9. Projected improvement in input referred noise – comparison between SPICE-simulations and hand calculations, after [3]. For large values of C<sub>2</sub>, hand calculations fail to capture other noise sources in the circuit.

### Acknowledgment

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