Radiometric Performance Enhancement of Hybrid and Monolithic Backside Illuminated CMOS APS for Space-borne Imaging

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Abstract

In this paper we discuss the development of high-end CMOS detectors whose radiometric performance has been optimized for space-borne imaging. This ESA development program [1] aims to demonstrate the advantages of CMOS APS in terms of system complexity, associated size and cost, added functionality and radiation tolerance, while offering the radiometric performance of scientific CCD based instruments. The design of the detectors has been discussed at the previous edition of this workshop [2]. This paper will focus on the measured results of the most important specifications and on the newly developed technology steps for the handling and processing of the thin device wafers.

1. Introduction

The aim of this ESA program is to improve the performance of CMOS APS to achieve CCD-like performance required for hyperspectral earth and planetary observation while adding well-known CMOS advantages like on-chip functionality, low power operation, high speed and radiation tolerance. The goal of such space missions is to observe parameters encompassing agriculture, forestry, soil/geological environ-ments and coastal zones/inland waters. These data can be used to improve our understanding of geospheric processes.

Important requirements for the sensor are snapshot operation to avoid image distortion due to the satellite's movement and high frame rates, combined with large dynamic range and high quantum efficiency. Therefore, the detectors combine some newly developed technologies to achieve the radiometric and functional performance that is required for the envisaged space applications. The pixel architecture allows for correlated double sampling combined with pipelined snapshot shutter for low noise and large full well operation. This is of particular interest for hyperspectral detectors or instruments operating in "step & stare" mode which would be compatible with high resolution and large dynamic range imaging systems, even in the case of microsatellites with low performance attitude and orbit control subsystem. High resolution earth observation instruments use preferably CCD TDI devices in pushbroom mode, requiring high satellite pointing stability. The use of 2D high resolution CCD arrays would require a mechanical shutter to stop integration during frame read out. This function is implemented at the device level with CMOS APS, simplifying the system design and eliminating shutter failure risk.

2. Sensor description

The detector architecture is shown in Figure 1. The pixel pitch is 22.5 μm in both X and Y direction. The readout sensor is processed in 0.35 μm Xfab technology, the diode arrays for hybridization were processed at Imec (0.13 μm technology).

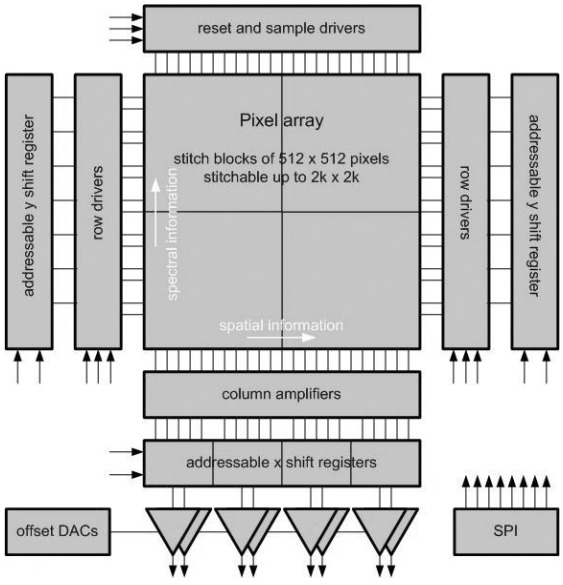
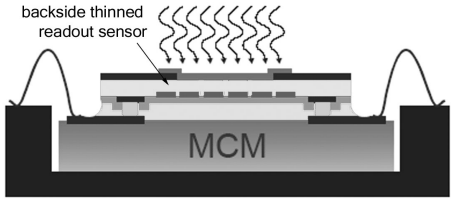
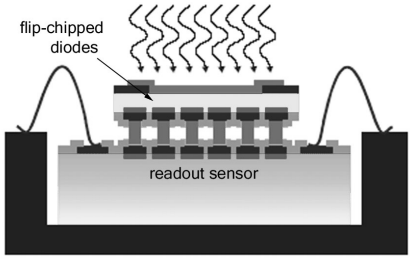


Figure 1. Sensor architecture.

Both required the stitching technique in which smaller blocks are repeated on the wafer. The pixel array consists of stitch blocks of 512 by 512 pixels and is stitchable up to 2048 by 2048 pixels. Columns are multiplexed in groups of 256 to a pseudo differential output (signal and reference output). Each output runs at a maximum readout frequency of 20 Mpixels/s.
Two types of backside-illuminated detectors are realized: either entirely monolithic or hybridized devices (Figure 2).



(a)



(b)

Figure 2. Monolithic backside illuminated approach (a) or hybrid sensor (b).

The pixel consists out of two stages: a light detecting stage and a sample and hold stage with three storage capacitors. This architecture, as explained in [1], allows for a true pipelined synchronous shutter with on-chip correlated double sampling (CDS), i.e. all pixels start and stop integration at the same moment while the previous frame is still read out.

The main pixel characteristics are given in Table 1. The pixel readout noise is determined by the size of the storage capacitors. The three capacitors, made by poly on diffusion, occupy about 70 % of the pixel area and equal each 350 fF. The photodiode capacitance is about 15 fF in case of the monolithic sensor and can vary from 25 fF to more than 1 pF in the hybrid approach.

Table 1. Measured sensor characteristics.

	monolithic	hybrid
in-pixel storage capacitance (fF)	350	350
full well charge (x 1000 electrons) (FWC)	> 200	> 950
conversion gain (uV/e)	6.93	1.45
dynamic range (FWC/dark noise) (dB)	75	75
maximum SNR (dB)	53	60

Both approaches have their advantages. The monolithic device requires less post-processing, leading eventually to the highest possible yield. Since its photodiode capacitance is as low as possible, it yields the best signal to noise ratio at low light levels. On the other hand, the hybrid approach allows for the highest flexibility in detector design (e.g. full well capacitance, cross talk reduction (see further)) and optimal shielding of the readout to avoid parasitic light sensitivity during readout.
Besides the normal operation mode with synchronous shutter and on-chip CDS, the sensor can also be programmed to read out the pixels non-destructively or to operate in a high dynamic range mode using a row dependent integration time [2].

3. Sensor processing

Innovative processing techniques on eight inch wafer scale have been developed and mastered which completely avoid the need for direct handling and processing of very thin (< 50 μm) wafers. All processing of thin device wafers (Figure 3) – including thinning – is performed on a temporary carrier, glued together with a temporary adhesive. The important advantage of this approach is that it allows the use of standard processing tools. Backgrinding, damage removal by dry and wet etching, implantation, laser annealing, deposition and resist patterning are all done on carrier wafer. Switching between backside and frontside processing of the thin wafers is made possible by a thin wafer transfer technique between carriers.
By means of a second adhesive, the initial wafer stack is glued to a second temporary carrier with the thin wafer facing towards the second carrier. Subsequently, the first carrier is removed, based on the different release properties of the adhesives. As a carrier, both Si and CTE matched SD2 glass have been used. Glass is used in case backside alignment with respect to the thin wafer frontside is required. CTE matching is needed to avoid thin wafer breakage on carrier while performing process steps at elevated temperature.

Fully processed thinned monolithic imagers are flip-chip bonded by means of large Au stud bumps on a redistributing MCM substrate (Figure 2). For hybridized imagers, in which the photodiode array is flip-chip integrated on the Read-Out IC, a single 10 μm diameter Indium bump per pixel is used. Both flip-chip operations have been done with and without carrier, although flip-chip without carrier is found to be more prone to die breakage. The bump interconnect yield was first assessed through daisy chain measurements and was found to be better than 99.98 %. In the final 1k x 1k hybrid demonstrators, the pixel functional yield of 99.93 % confirms these measurements.

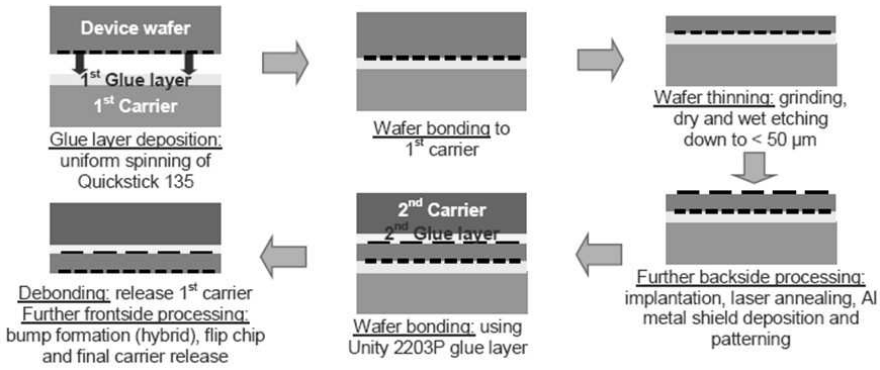


Figure 3. New thin eight inch wafer handling process flow for the fabrication of the thin imagers.

4. Measurement results

Since the readout time can be large compared to the integration time, the shutter efficiency is a key parameter. It has been measured to be virtually 100 %, certainly for the hybrid detectors where the pixel storage elements are completely shielded due to the bump interconnect.

Also the quantum efficiency is of utmost importance for the envisaged applications. The QE of the detectors has been optimized for the range of 400 to 850 nm, resulting in a final epi thickness of about 22 to 35 µm for the monolithic and hybrid devices respectively. A one-dimensional analytical model was developed to calculate the propagation and absorption of an incoming wave in the layer stack: air, anti-reflective coating (or without), the silicon epi layer and the dielectrics on the frontside. The epi layer includes a shallow boron implanted region for which it is assumed that all charges generated in this region will recombine and be lost for collection (i.e. dead layer). The surface recombination velocity at the border of this layer was empirically determined from the various QE measurements. Furthermore, the highly doped region has a sloped doping profile of about 75 nm. The backside surface field created by this implant profile is taken into account in the model, as well as the internal electric field generated by the varying epi doping profile [2]. Figure 5 shows the measurements of the QE on a 1k x 1k monolithic device without ARC. The measurements are in close agreement with the simulation where a 15 nm dead layer thickness is used (the ideal case of no dead layer is shown as reference). Recently, the following experiment has been carried out. A laser annealed device yielding good quantum efficiency over the full wavelength range, underwent an oxide plasma clean step. This process re-introduced surface damage resulting in large charge carrier recombination. The figure shows that the damage was nearly completely annealed by a single laser pulse (SP), but that a larger number of laser pulses again increases the surface damage, and consequently reduces the quantum efficiency, especially in the short wavelength range.

Reflectivity measurements of an optimized ARC, consisting of a ZnS/MgF_2 stack, have shown less than 3 % light loss in the range of interest (Figure 4). Application of this ARC on the devices as measured in Figure 5 thus gives a global QE well above 80 %.

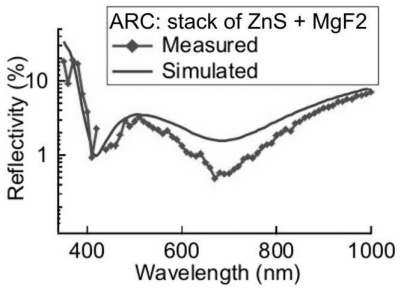


Figure 4. Optimized ARC properties. Global reflective light loss is less than 3 % over the extended optical range of interest (400-850 nm).

Typically, to optimize the epi thickness, there is a trade-off between cross talk on one hand and quantum efficiency and sensitivity (small photodiodes) on the other hand. This can be partially alleviated by using high resistivity substrates and/or large bias voltages. However, large depletion would lead to increased dark current and unwanted susceptibility to proton displacement damage. Therefore, in both the hybrid detectors and the monolithic sensors, a varying epi doping profile results in a built-in electric field that will accelerate the collection of photo-generated charges and improve the cross talk behaviour [2][3]. The dark current of a monolithic device was measured to remain below 3000 electrons/s at room temperature after subsequent irradiation by $5x10^{10}$ protons/cm^2 and 50 krad(Si) from a Co^{60} source.

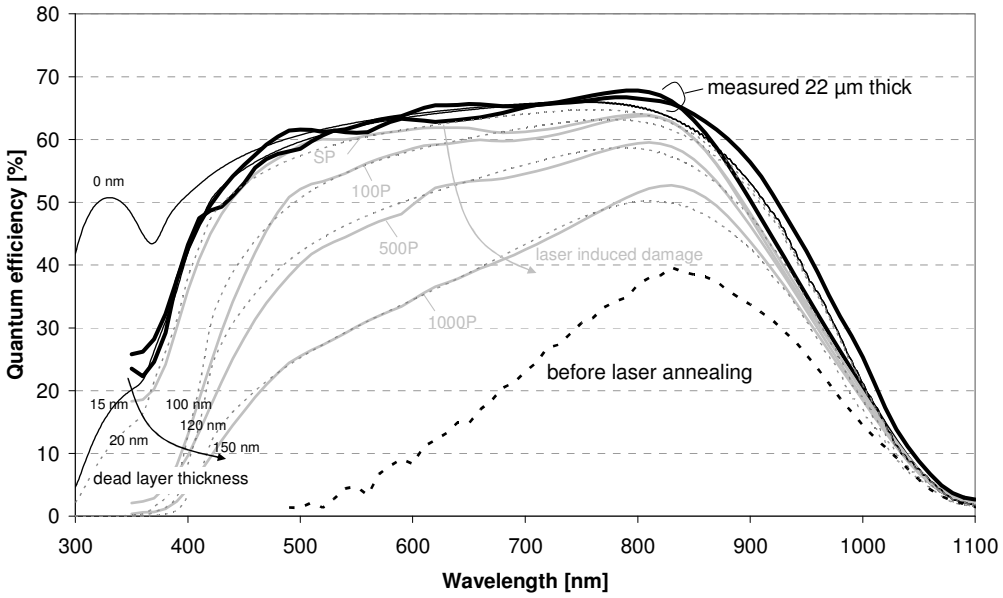


Figure 5. Measured and simulated quantum efficiency curves before and after backside treatment. A non-optimized laser anneal process will also lead to increased surface recombination.

In a hybrid detector, the cross talk due to diffusion has been eliminated completely through highly doped polysilicon filled trenches with high aspect ratio (Figure 6). These 1 µm wide 50 µm deep trenches confine the collection volume to individual pixel and enforce a lateral drift field between pixels. Quantitative measurements of the cross talk in the detectors are currently being carried out.

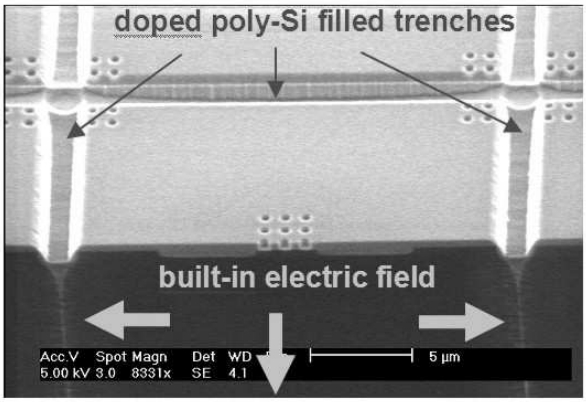


Figure 6. Top view and cross section of a single 22.5 µm pitched pixel surrounded by trenches (diodes for hybridization before metallization step).

5. Conclusions

In this paper we presented the development of a CMOS image sensor that is targeted towards space-borne imaging applications like hyperspectral imaging. The pixel is characterized by the implementation of three storage capacitors, which allow for a synchronous pipelined shutter operation, combined with CDS on-chip. The readout sensor can be used either as readout chip for hybridized diodes or as monolithic backside illuminated device. Innovative processing techniques on eight inch wafer scale have been developed to avoid any direct handling and processing of thin wafers by the use of temporary carrier wafers. This allows us to use only standard process tools. A number of techniques and performance enhancing concepts (like the use of graded epi and pixel isolating trenches) have been combined. To the authors' knowledge, the combination of this graded thick epi and cross talk reducing trenches makes these backside illuminated CMOS detectors unique.

References

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[3] B. Dierickx, J. Bogaerts, "NIR-enhanced image sensor using multiple epitaxial layers", Electronic Imaging, San Jose, 21 Jan 2004; SPIE Proceedings vol. 5301, p. 204, 2004.