Trends in CMOS Imager Technology for Low Power and Low Cost Applications

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Image sensor design faces an ever-increasing challenge due to the scaling down of the pixel area in an effort to reduce chip production costs while increasing device spatial resolution. Although many circuit design techniques have been developed and many more will be required as the pixels are scaled down, the fundamental limits of performance are related to the design and structure of the unit pixel itself.

New and improved methods of packing photodiodes closer together while maintaining sensitivity and without increasing noise are beginning to emerge as the industry moves to active pixel sensor sizes below 2µm [1]. One of the most important aspects of pixel scaling is engineering of the photodiode and related active areas in the silicon substrate. Other groups have studied photodiode design through careful simulation work [2], [3]. Through our consulting work benchmarking CMOS image sensors, we have found that Scanning Capacitance Microscopy (SCM) is an absolutely indispensable tool for providing a complete understanding of production samples.

Traditional SEM imaging techniques provide the best overall view of the various materials and processes used in modern CIS fabrication. This can be seen in a topographical view of one manufacturer's APS design and cross-section in Figure 1. However, SEM cannot extract details of the photodiode and other aspects of substrate design. The SCM views of one manufacturer's recent (2.7µm pixel generation) APS design and structure are shown in Figures 2 through 4.

Other scanned probe techniques are also very valuable in the study of CIS fabrication. Atomic Force Microscopy (AFM) can be used to evaluate the important back end processes of color filter and microlens arrays. SEM imaging may not provide sufficient detail about the final structure. There are several recent articles describing techniques for denser packing of the microlens such as dead zone free [4] or zero gap [5]. Figures 5 through 8 show examples of AFM providing insight into lens and filter height, shape and uniformity.

As APS dimensions shrink, signal-to-noise ratio is reduced. In our work, we have begun to see production devices that employ structures to avoid structures that contribute to the total device noise. One of these is shallow trench isolation (STI). There has been a migration toward more junction isolation (Figure 3) and field oxide above the substrate rather than in the usual STI approach. We predict that there will be increased emphasis on keeping the substrate design interface free whenever possible.

In conclusion, we have used AFM and SCM to examine the current state-of-the-art in commercial CMOS image sensors from the leading manufacturers. These analytical techniques reveal a great deal about the final photodiode and associated substrate design. We believe that our benchmarking and predictive trends studies suggest the use of AFM and SCM more extensively in the development of the next generation of CMOS image sensors.

[1] K. Itonaga, H. Abe, I. Yoshihara, and T. Hirayama, “A High-Performance and Low-Noise CMOS Image Sensor with an Expanding Photodiode under the Isolation Oxide,” 33.1, Technical Digest of the 2005 IEEE International Electron Devices Meeting
[2] Igor Shcherback, Tatiana Danov, and Orly Yadid-Pecht, “A Comprehensive CMOS APS CTK Study: Photoresponse Model, Technology, And Design Trends,” IEEE Transactions on Electron Devices, Vol. 51, No. 12, December 2004
[3] Igor Shcherback, Tatiana Danov, and Orly Yadid-Pecht, Study of CMOS APS Responsivity Enhancement: Ring-Shaped Photodiode, IEEE Transactions On Electron Devices, Vol. 52, No. 1, January 2005
[4] Young Chan Kim et al, “1/inch 7.2 mega-pixel CMOS Image Sensor with 2.25um Pixel Using 4-shared Pixel Structure for Pixel-level Charge Summation,” Proceedings of the 2006 IEEE International Solid-State Circuits Conference
[5] M. Cohen et al, “Fully Optimized Cu based process with dedicated cavity etch for 1.75µm and 1.45µm pixel pitch CMOS Image Sensors,” 5.4, Technical Digest of the 2006 IEEE International Electron Devices Meeting

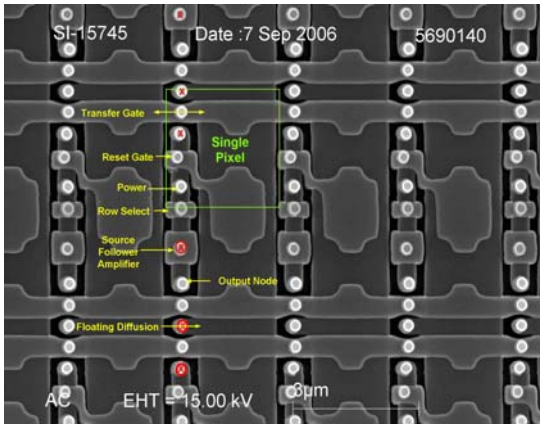

Figure 1: SEM micrograph of APS design at polysilicon level (manufacturer A, 2.7µm APS)

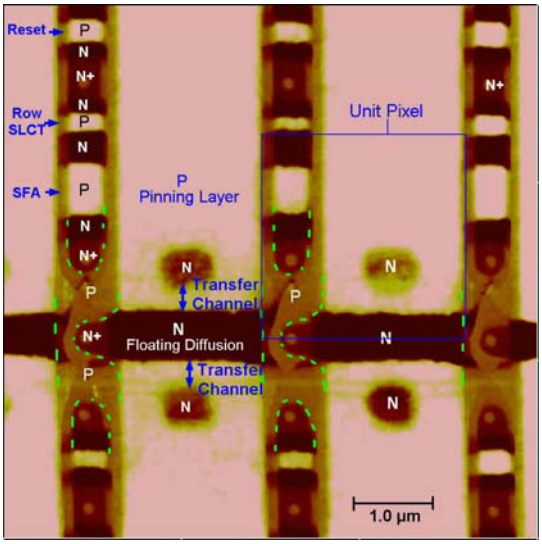

Figure 2: SCM 2D map of APS design at diffusion level (manufacturer A)

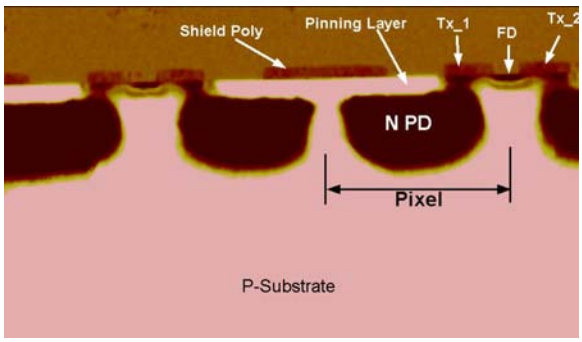

Figure 3: 2D cross-section SCM map of photodiode structure (manufacturer A)

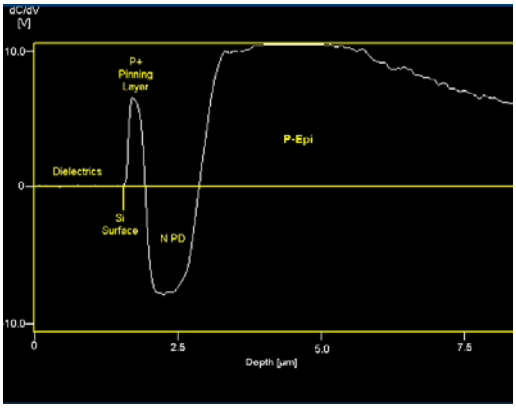

Figure 4: 1D SCM linescan of junction depths in photodiode region (manufacturer A)

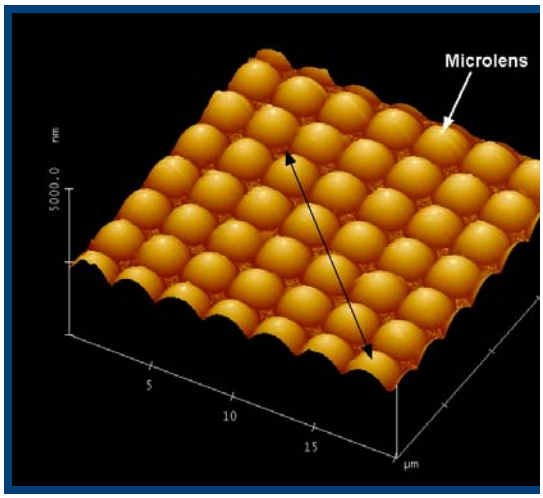

Figure 5: AFM image of microlenses (angle view) (manufacturer B)

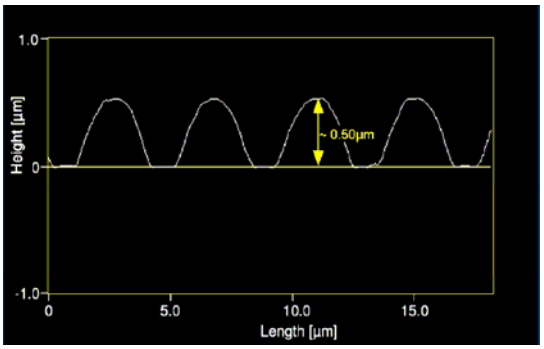

Figure 6: AFM line profile of microlenses (manufacturer B)

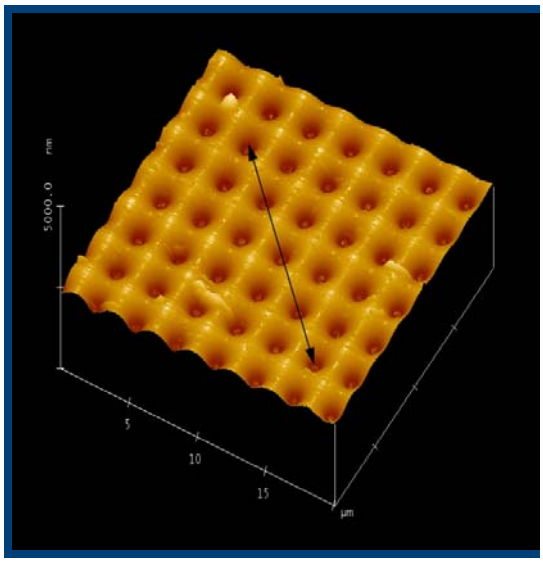

Figure 7: AFM image of blue filter covering periphery (angle view) (manufacturer B)

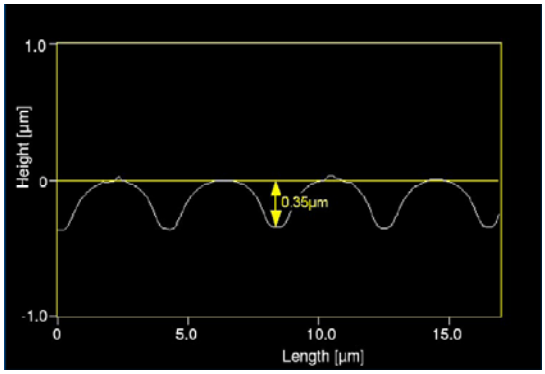

Figure 8: AFM line profile of blue filter covering control circuits (manufacturer B)

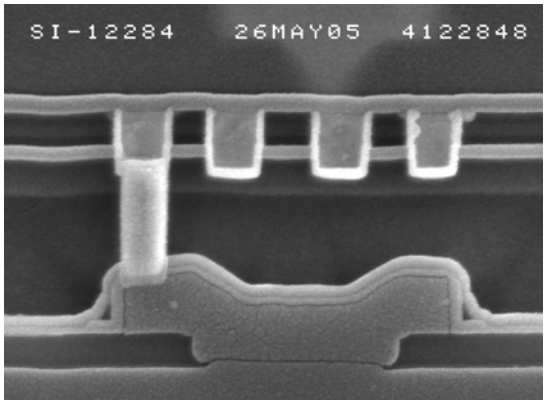

Figure 9: Deposited field oxide isolation (manufacturer C, 2.5µm APS)