

# Dynamic range extension of CMOS imager with linear response by hybrid use of active and passive pixel readouts

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## ABSTRACT

We present a new dynamic range extension method of CMOS imager by hybrid use of active and passive pixel readout methods with electrical calibration for image reproduction. Based on a CMOS imager with a lateral overflow integration capacitor, we have introduced the passive pixel readout to reading the charges in the overflow capacitor for high illumination to achieve high linearity, wide dynamic range more than 120dB, and no moving image deterioration as well as high-sensitivity given by the active readout. We have fabricated a 128x96-pixel prototype image sensor in a 0.35- $\mu\text{m}$  CMOS technology. In this paper, we demonstrate image acquisition by the prototype sensor, and show offline image reproduction to enhance the dynamic range by 18.5dB with electrical calibration. After image reproduction, column fixed pattern noise in the passive readout was reduced from 10.6%rms to 0.97%rms.

## I. INTRODUCTION

CMOS imagers are promising in wide dynamic range image acquisition due to their capability of integrating various kinds of electronic circuits. In this paper, a new dynamic range extension method of CMOS imager by hybrid use of active and passive pixel readouts with electrical calibration for image reproduction is presented. A CMOS imager with a lateral overflow integration capacitor[1] provides high-sensitivity, linearity, and wide dynamic range around 100dB, and is free from moving image deterioration, which is a significant problem in multi-sampling methods[2]. We propose to utilize the passive readout method[3] to read the overflowed photocharges, and demonstrate acquisition of the reproduced images with a prototype sensor. By use of the advantage of the passive readout method such as large charge capacity, available voltage range of the overflow capacitor can be increased to further extend the dynamic range. The amount of the saturation charges can be several times as much as that by the active readout method. Moreover, nonlinear region of the MOS capacitor as an overflow capacitor can be utilized without degrading the linearity to maximize the dynamic range. In this paper, we show a 128x96-pixel prototype image sensor fabricated in a 0.35- $\mu\text{m}$  CMOS technology, and demonstrate image acquisition by the prototype sensor. We show offline image reproduction to enhance the dynamic range with electrical calibration, and demonstrate that our image reproduction method has effect of reducing column fixed pattern noise (FPN) in the passive readout.

## II. CMOS IMAGER BASED ON HYBRID PIXEL READOUT ARCHITECTURE

Figures 1 and 2 show the pixel structure and an example of the potential diagram. The pixel has a MOS capacitor as an overflow capacitor ( $C_{\text{OF}}$ ), overflow-control transistor ( $M_{\text{OF}}$ ), an anti-blooming transistor ( $M_{\text{AB}}$ ), source follower transistor ( $M_{\text{SF}}$ ) for active readout, and select transistors for active and passive readouts ( $M_{\text{RSA}}$  and  $M_{\text{RSP}}$ ). The procedure for readout of each pixel is composed of 1) non-destructive active readout of the photodiode potential, 2) decision of the actual readout mode based on the non-destructive readout result, and 3)

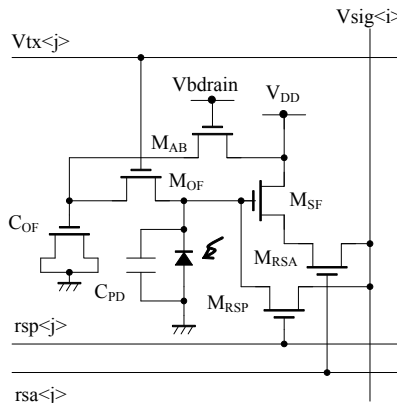


Fig. 1. Pixel schematic.

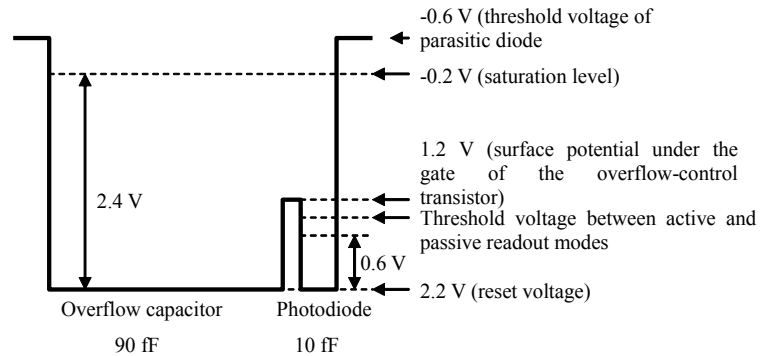


Fig. 2. Simplified potential diagram for explaining dynamic range extension by the proposed method.

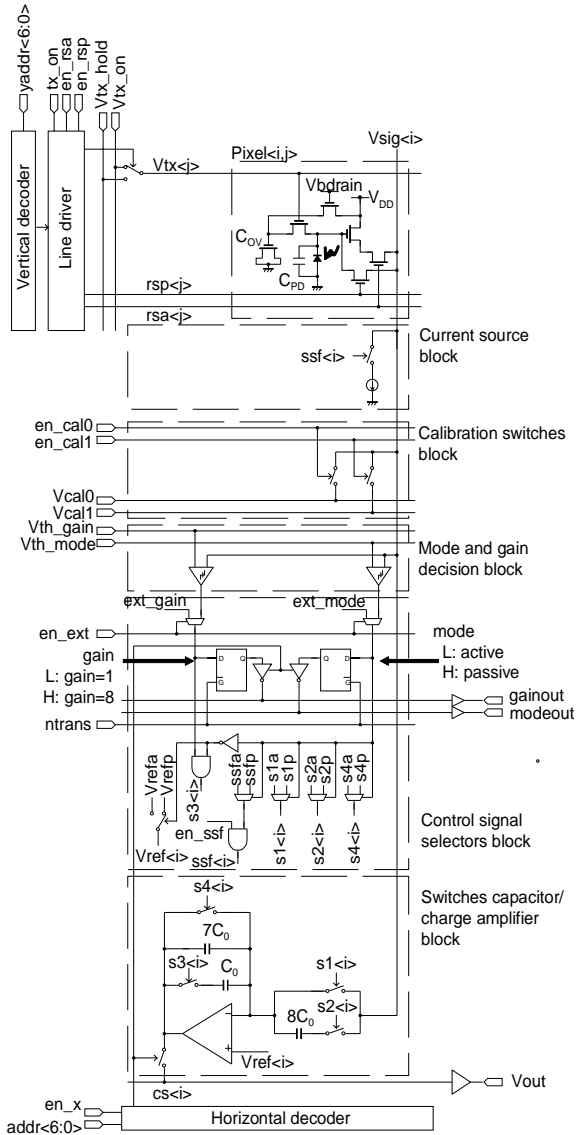


Fig. 3. Pixel structure and a simplified schematic of the CMOS imager.

actual pixel readout and reset. The actual readout for the active or passive readout is performed by use of a switched capacitor amplifier or a charge amplifier, respectively. As shown in Fig. 2, the advantage of the passive readout is large charge capacity given by large overflow capacitance and large voltage range whose lower limit is smaller than the threshold voltage of the select transistor  $M_{RSP}$ . We can utilize the voltage range under the threshold of the switch transistor and even under 0 V, which increases the amount of the saturation charges, and enlarges the dynamic range. Another advantage is good linearity due to usage of the charge amplifier, while the capacitance of the MOS capacitor is highly nonlinear under the threshold voltage.

Figure 3 and Table 1 show the simplified schematic of the CMOS imager and its specifications, respectively. To select pixel readout methods, passive or active, according to the illumination pixel by pixel, the pixel has two readout paths to the vertical signal line of each column. One of paths is composed of a source follower transistor and a switch transistor for active readout, and the other is only a switch transistor for passive readout. Readout mode is determined by the source follower output of the non-destructive active readout followed by the actual readout. The column amplifier works as a switched capacitor in the active readout mode or a charge amplifier in the passive mode.

Figure 4 and Table 2 show a timing chart for one horizontal period and operations for each elemental period, respectively. At first, source follower output by a non-destructive active readout is compared with the predetermined threshold voltage, and the readout mode is determined. Then, pixel readout is executed in the appropriate readout mode at each column. Note that row control signals such as  $rsa<j>$ ,  $rsp<j>$ , and  $tx\_on<j>$  are shared in a row. To avoid the conflict of pixel operation between two readout modes, no operation (NOP) is

Table 1. Specifications and characteristics of the prototype sensor.

Technology	0.35- $\mu$ m standard CMOS (2P, 4M)
Chip size	4.5 mm x 8.2 mm
Pixel size	15 $\mu$ m sq.
Components in pixel	1 PD, 5 transistors, and 1 MOS capacitor
Pixel count	128 $\times$ 96
Frame rate	30 fps
Sensitivity	3.3 V/lx $\cdot$ s (APS) 0.036 V/lx $\cdot$ s (PPS)
Dynamic range	54.3dB (APS)/ 45.7dB(PPS)
Dynamic range extension by PPS	18.5dB
Total dynamic range	72.8dB
Column FPN	0.28%rms (APS)/ 10.6%rms (PPS before mapping)/ 0.97%rms (PPS after mapping)
Pixel FPN	0.64%rms (APS)/ 0.10%rms (PPS before mapping)/ 0.55%rms(PPS after mapping)

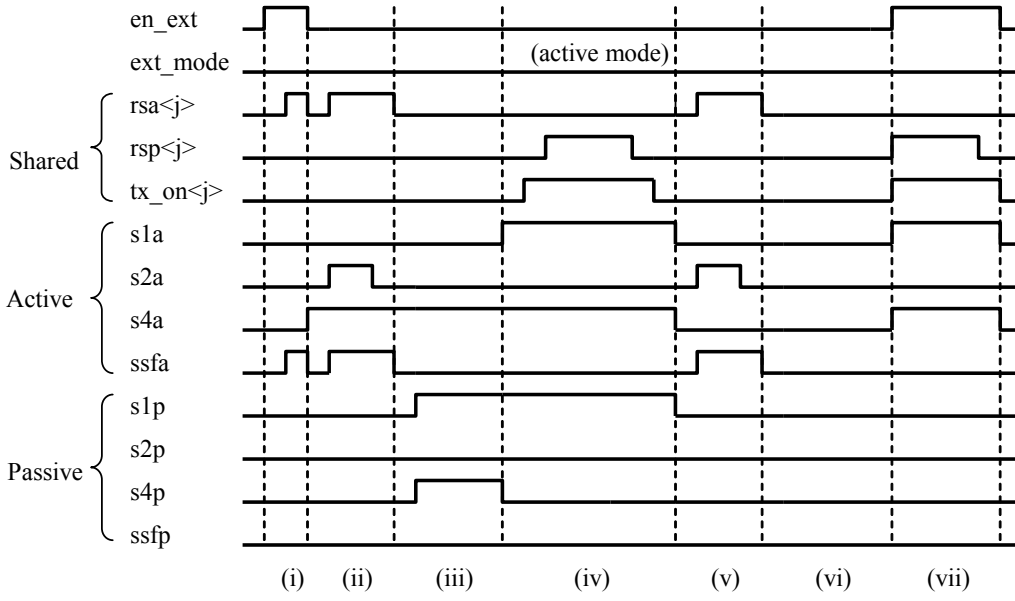


Fig. 4. Timing chart.

Table 2. Operations in one horizontal period.

Period	(i)	(ii)	(iii)	(iv)	(v)	(vi)	(vii)
Active	mode and gain decision	auto-zeroing	NOP	pixel reset	amplification	readout off-chip	pixel reset
Passive		NOP	auto-zeroing	amplification	NOP		

properly inserted in the pixel readout procedure.

In the case of the configuration shown in Fig. 3, dynamic range can be extended by 32dB at most with the passive readout. Disadvantage of the passive readout is large noises concerning the capacitance of the vertical signal line is suppressed in our sensor because the feedback capacitance  $C_0$  of the charge amplifier is comparable with the parasitic capacitance of the vertical signal line to extend the dynamic range.  $C_0$  is 100fF in this case.

### III. EXPERIMENTAL RESULTS

Table 1 summarizes the characteristics of the prototype imager. Figure 5 shows relationship between illumination and the voltage of the sensor output. The dynamic range is enhanced by 18.5dB with the passive readout.

The sensor has calibration switches that can supply test voltages directly to the photodiode in a pixel. By use of the sensor outputs for two different test voltages in two readout modes, the outputs by the passive mode can be mapped on the active outputs. The mapping function is given by the following equation.

$$V_{out,A} = \frac{V_{A1} - V_{A2}}{V_{P1} - V_{P2}} \cdot V_{out,P} + \frac{V_{P1}V_{A2} - V_{P2}V_{A1}}{V_{P1} - V_{P2}}. \quad (1)$$

The readout result in the passive mode,  $V_{out,P}$ , is mapped on  $V_{out,A}$ .  $V_{A1}$ ,  $V_{A2}$ ,  $V_{P1}$ , and  $V_{P2}$  are the outputs of the imager for the test voltages of  $V_{cal0}$  and  $V_{cal1}$ . Note that  $V_{cal0}$  and  $V_{cal1}$  do not appear in Eq. 1.

As shown in Fig. 5(b), we can see that the passive outputs can be successfully mapped on the line of the active outputs.  $V_{cal0}$  and  $V_{cal1}$  were 1.6 V and 2.1 V, respectively. Figure 6(a) and (b) show the captured images in active and passive readout modes, respectively. Figure 6(c) and (d) show the operation mode for each pixel and the reproduced image with off-line processing. They were calculated from the images in Fig. 6(a) and (b) and four images for two test voltages read out in the active and the passive modes. As shown in Fig. 6(d), the dynamic range has been successfully enlarged. Image reproduction mapping given by Eq. 1 enables us to decrease the FPN in the passive readout because the information of the FPN is included in the mapping functions. As shown in Table 1, column FPN was reduced from 10.6%rms to 0.97%rms after the image reproduction. Note that the mapping function given by Eq. 1 was obtained for each pixel in the offline processing because that was a preliminary demonstration. However, in the goal, the mapping function is acquired for each column because pixel-wise FPN is eliminated by the column amplifier.

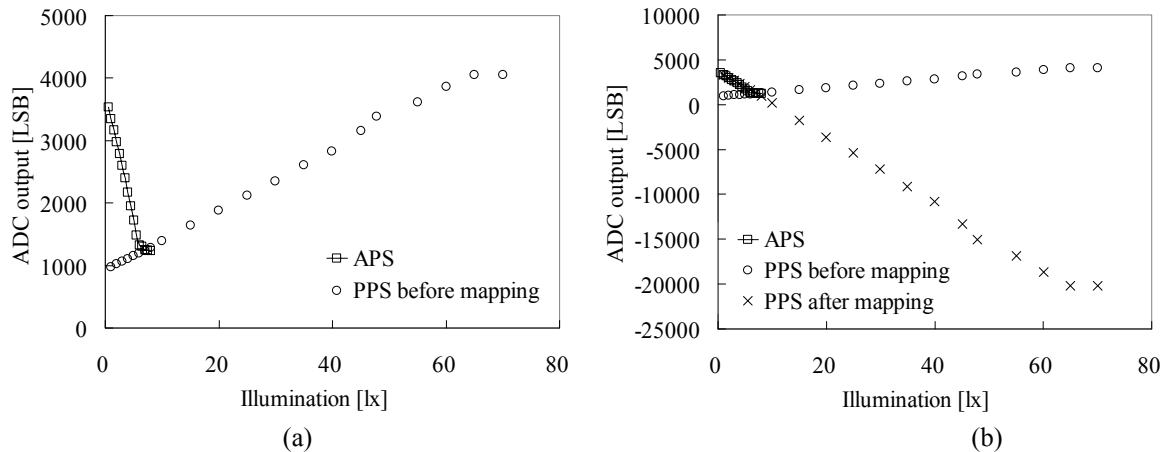


Fig. 5. Relationship between illumination and sensor outputs (a) before and (b) after reproduction mapping.

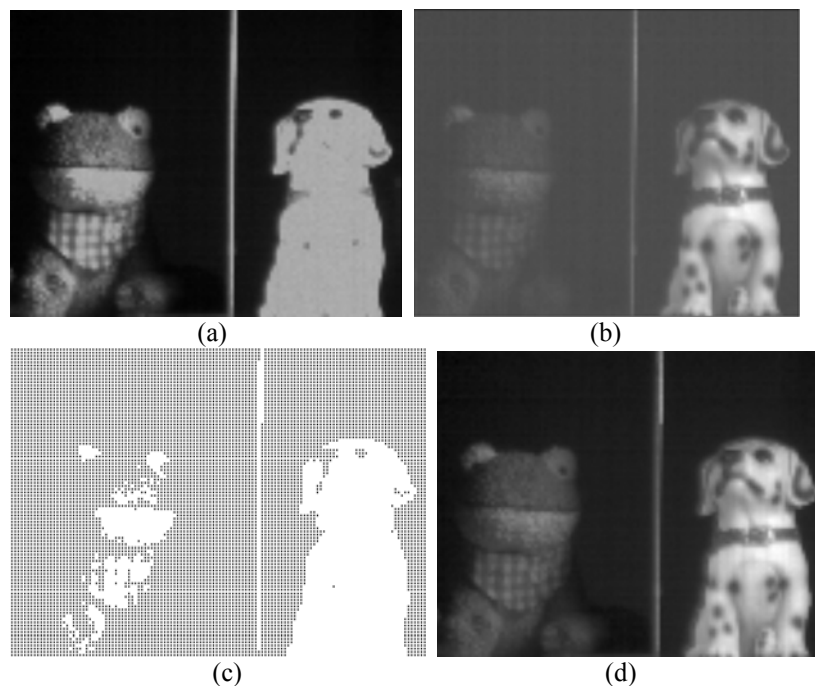


Fig. 6. Captured images by (a) APS and (b) PPS modes ( $\gamma=1.0$ ), (c) operation modes of each pixel (black: active, white: passive), and (d) off-line reproduced image with enhanced dynamic range ( $\gamma$  was controlled with 2.0). Only column CDS is performed on the sensor.

#### IV. CONCLUSIONS

We have proposed dynamic range extension by hybrid use of active and passive readout methods. We have fabricated a 128x96-pixel CMOS imager with the proposed scheme in a 0.35- $\mu\text{m}$  CMOS technology. From the experiments, image reproduction and dynamic range extension of 18.5dB have been successfully demonstrated.

The dynamic range will be increased by up to 32dB by optimizing the feedback capacitance of the charge amplifier (400 fF). Total dynamic range can be enlarged to about 120dB, which is required in the automotive applications, with an adaptive gain method [4]. By use of 0.18- $\mu\text{m}$  CMOS technology, the pixel size will be shrunk to about 5  $\mu\text{m}$  sq without decreasing overflow capacitance.

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