

# Comparison of Global Shutter Pixels for CMOS Image Sensors

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## Abstract

In this paper we are presenting preliminary results from 4T technology based CMOS image sensors with global shutter, i.e. all pixels in the active array integrate light simultaneously. The global shutter operation mode is particularly important for high-speed video applications, where the more commonly implemented rolling line shutter creates motion blur. Our chips were fabricated using a 0.18 micron 4T, CIS technology with pinned photodiode and transfer gate. Different from conventional 3T type CMOS image sensors with global shutter pixel, in these 4T technology based global shutter pixels, the charge is transferred, not just sampled, onto the sense node. This translates into very high sensitivity and low readout noise at low power. For an imager with 7 transistors per pixel that is operated in global shutter, “Integrate While Read” mode, we measure an input referred noise of 10 electrons. The extinction ratio at full well signal charge is  $\sim 97.7\%$ .

## 1. Introduction

Electronic exposure time control is a standard feature in digital still picture and video cameras, and for many applications this feature can be integrated directly into the sensor, eliminating the need for an external shutter mechanism. In CMOS image sensors (CIS) there are two fundamentally different shutter implementations, i.e. rolling line or global shutter. Due to the lower transistor count per pixel, the rolling line shutter has been the standard approach for electronic exposure time control in monolithic visible CMOS image sensors. Although a rolling line shutter imager (RLSI) can provide a very short integration time, artifacts are created when imaging fast moving scenes because each line of pixels is integrating light at a slightly different moment in time. For a RLSI the minimum possible scene time, defined as period between light integration in the first row of pixel to integration in the last row of pixel, is the frame readout time. This frame readout time can be much longer than the exposure time, required to image a fast moving scene without artifacts.

Over the past years pixels have become so small, that the true imager resolution is becoming defined by the fundamental optical diffraction limit [1]. Further shrinking of minimum feature size can therefore be applied to integrate more functionality, f.e. a global shutter, which requires a higher transistor count per pixel. Also, a reduction in the “as drawn” fill factor of a pixel is less critical to achieve maximum light

sensitivity, due to the availability of micro lenses and the arising possibilities of backside illumination for CMOS image sensors. Only the full well capacity is reduced by the potentially smaller size of the photodiode. However, a GSI camera with global shutter imager is especially operated at short integration times, i.e. low effective signal levels, and maximum light sensitivity, defined by the sense node capacitance, is typically more important than full well capacity.

Therefore in order to maximize light sensitivity, low readout noise is particularly important in GSI cameras. However, a conventional 3T technology is not very well suited for 3 reasons: 1. Charge can only be shared between the photodiode and the sense node so that there is no voltage gain [2], 2. kTC noise can only be reduced by partial reset techniques like soft reset that are inherently prone to image lag which is not acceptable in high speed cameras, 3. kTC noise from photodiode and sense node reset, respectively contribute independently to the total noise, leading to a factor  $\sqrt{2}$  higher noise compared to rolling line shutter imagers with the same full well capacity. These drawbacks cause lower light sensitivity but can be overcome by using a 4T process with pinned photodiode. Some operating constraints may still apply, depending on the number of transistors per pixel. For example, when using a CMOS image sensor process with pinned photodiode and transfer gate, a 4 or 6 transistor pixel can only be operated at moderate photon flux levels where the photodiode

full well capacity is large enough to integrate all photo charge carriers that are generated during the readout period. But many GSI sensors are operated under very strong lighting conditions, where the photon flux level exceeds the available full well capacity many times, causing image ghosting from shutter leakage. Fundamentally no such constraints exist for pixels with 7 transistors, although shutter leakage is critical in any monolithic GSI sensor [2].

4T type pixels with rolling line shutter have already been demonstrated to deliver very low noise [3]. We analyzed the performance of GSI sensors with 4, 5, 6 and 7 transistors per pixel, based on a 0.18 micron CIS technology with pinned photodiode and transfer gate. In addition to standard 4T CIS technologies, CCD type electrodes are available in this process for noise free charge domain signal processing. Our results are summarized in the following section. Initial results confirm the low noise capabilities of such pixels for applications in global shutter CMOS image sensors.

## 2. Results

The goal of our designs was the development of a low noise global shutter pixel for operation in “Integrate While Read” (IWR) mode, i.e. the 7T pixel. Consideration of 4, 5, and 6T pixels is for reference only. An overview of global shutter pixels is given in figure 3. The 4T ITR pixel was listed for completeness, but was not tested, because it is not compatible with 4T process technology. All pixels were integrated on a test imager with analog output and have a size of 8x8 micron<sup>2</sup>. 12bit digitization is provided off-chip using a customized in-house readout board.

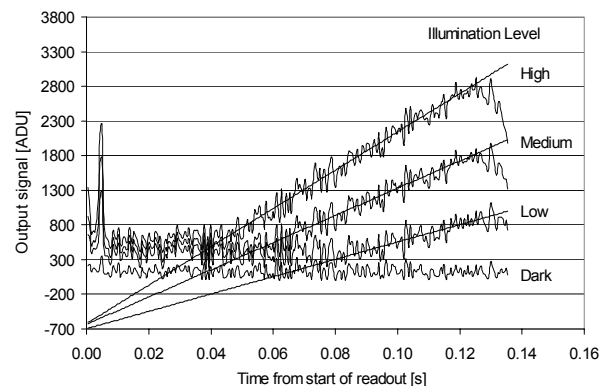


Figure 1: Output signal as a function of delay time between end of shutter gate pulse on TG and readout time

At low illumination levels, a 4T IWR pixel can be operated in global shutter mode, although it can only be read out using double sampling, i.e. not correlated double sampling. At higher illumination levels the shutter does not block light from parasitic charge integration on the sense node, because no proper charge drainage is provided on the photodiode. The same applies to the 6T pixel, which was qualitatively confirmed by not clocking the RsPD transistor in the 7T pixel. Figure 1 shows the output signal as a function of delay time between setting the shutter transistor TG to zero and the beginning of the readout for the 4T IWR pixel. As soon as the photodiode capacity limit is reached the transfer gate does not isolate the PPD from SN anymore. Because the signal charge per frame usually exceeds the available full well capacity, the 4T and 6T pixels will perform poorly in any practical GSI camera application.

For a global shutter pixel with pinned photodiode and transfer gate the maximum achievable frame rate is determined by the time that it takes to remove the signal charge from the photodiode onto the sense node. We measured this time for a 4T IWR pixel by modulating the pulse width of the transfer gate pulse, TG. The measurement results are shown in figure 2. From this measurement it can be concluded that the charge transfer is complete after ~10 micro seconds in these pixels. The longer decay time of this response curve can be attributed to the RC time constant on the TX node after it is switched back to zero.

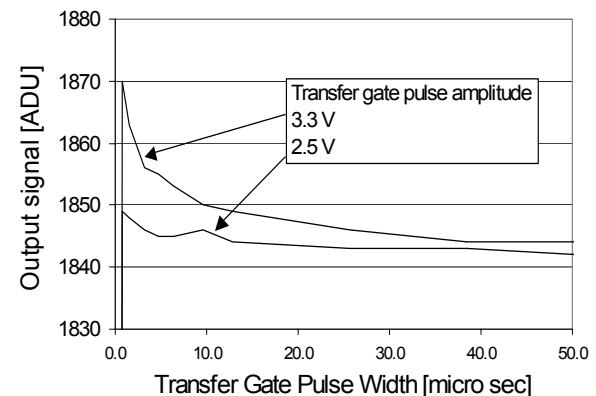


Figure 2: Output signal as a function of transfer gate pulse width for TG pulse amplitudes of 2.5V and 3.3 V, respectively

Although the presented 4T pixel does not perform well in global shutter imagers due parasitic charge integration on the storage node, the results of this characterization produce valuable insight into how photo generated charge carriers can reach the sense node SN.

#1		4T	<p>Integrate while read (IWR)          Double Sampling (DS) readout          Only suited for low photon flux levels          kTC noise limited          FWC defined by PPD or SN capacity          Measured: 2.75 e<sup>-</sup> noise in rolling line shutter mode          ~30 e<sup>-</sup> in global shutter mode</p>
#2		4T	<p>Integrate Then Read (ITR)          Double sampling (DS) readout combined with global reset and signal sampling          Suited for high photon flux levels          kTC noise limited          FWC defined by PD capacity          Signal sampling onto SN          (not possible with PPD+TG technology)          Estimated: ~30e<sup>-</sup> if PD has similar FWC as PPD in pixel #1</p>
#3		5T	<p>Integrate while read          Double sampling readout          Suited for high photon flux levels          kTC noise limited          FWC defined by PPD or SN capacity          Charge transfer onto SN          (based on PPD+TG technology)          Estimated: ~30e<sup>-</sup> if SN has same dimensions as pixel #1</p>
#4		6T	<p>Integrate then read          Correlated Double Sampling (CDS readout)          Only suited for low photon flux levels          kTC noise free          FWC defined by PPD, SH or SN capacity          Charge transfer onto SN          Same performance as pixel #5 when RsPD kept at zero</p>
#5		7T	<p>Integrate While Read (IWR)          Correlated Double sampling (CDS readout)          Suited for high photon flux levels          FWC defined by SH and SN capacity          Charge transfer onto SN          Measured: 10 e<sup>-</sup></p>

PPD - Pinned Photo Diode  
 PD - Photodiode  
 TG - Transfer Gate  
 SH - Sample Hold Gate  
 SS - Sample Signal Gate  
 FWC - Full Well Capacity

SN - Sense Node  
 RsPD - Reset Photodiode  
 RsSN - Reset Sense Node  
 SF - Source Follower  
 RD - Read

Figure 3: Overview of global shutter pixels. The 5T and 7T pixels can be operated in “Integrate while Read” mode. Correlated Double Sampling (CDS) readout is only possible for a 6T and 7T pixel

Using the same 0.18  $\mu\text{m}$  CMOS process, a global shutter imager with 7T IWR pixel was fabricated. For characterization the chip was mounted in a camera like setup and basic imaging performance was demonstrated. For all further measurements the lens was removed and the sensor was illuminated with a white light source. No IR radiation filter was applied. In order to measure the temporal noise, we recorded the standard deviation as a function of signal intensity in the shot noise limited domain for a single pixel. The slope of this curve represents the sensitivity in  $\text{ADU}/e^-$ . Using the conversion factor of  $0.5 \text{ ADU}/e^-$ , the input referred noise in number of electrons was measured to be  $10e^-$ . The noise measurement for the 7T pixel is presented in figure 4. In this measurement the signal level was modulated via integration time and light intensity, respectively. Both methods result in the same noise level for the same input intensity.

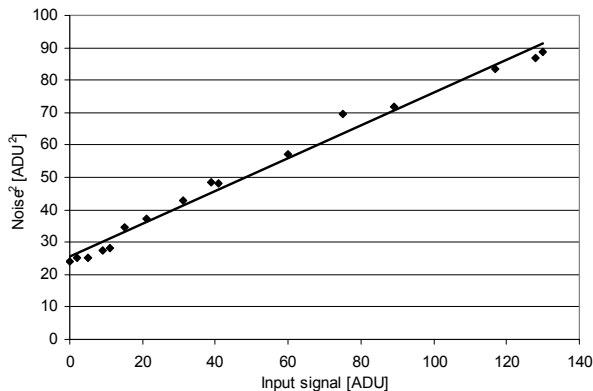


Figure 4:  $\text{Noise}^2$  versus input signal. From RMS line fit: sensitivity =  $0.5 \text{ ADU}/e^-$ , readout noise =  $10 e^-$

## References

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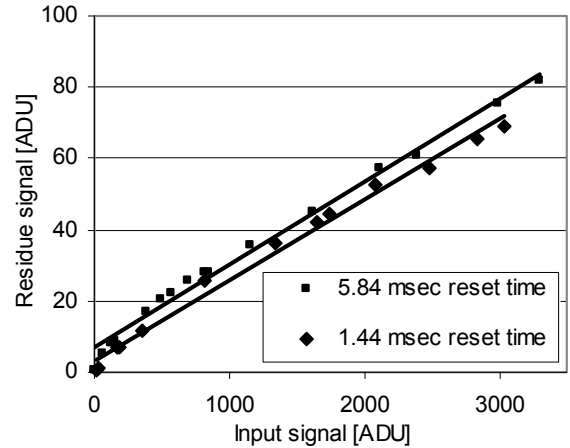


Figure 5: Residue Signal as a function of input signal after TX gate in pixel #7 is switched to zero

## 3. Summary

Based on a 7 transistor pixel with pinned photo diode and transfer gate, we demonstrated a global shutter imager with a temporal readout noise of  $10e^-$  for an  $8 \times 8 \text{ micron}^2$  pixel in  $0.18 \mu\text{m}$  CMOS technology. This noise level is slightly higher compared to that in a conventional rolling line shutter CMOS image sensor with comparable sense node capacitance. The shutter leakage of 2.3% for this pixel is comparatively high and is attributed to diffusion of photo generated charge carriers onto the sense node. Some improvements will be possible from modified timing and by inserting and NIR filter into the optical path. However, the main improvement is expected from modifications in the underlying CIS process.