A High Speed 4 Megapixel Digital CMOS Sensor

Alex Krymski

Alexima, 1028 N Lake Suite 204, Pasadena, CA 91104, USA
krymski@alexima.com

Abstract

We developed, fabricated and characterized a shuttered 4 Mpixel digital CMOS sensor running at the rate over 400 Frames/s. This paper discusses the pixel, the column ADC and the data readout architecture. The sensor delivers over 1.8 GPix/s of data at the maximum clock rate of 120 MHz. We also discuss the techniques implemented in the chip to reduce electronic noises.

The closest published sensor is a 4 Mpixel sensor developed by Photobit Technology [1], and which has become a popular product to machine vision and motion capture industries. The chip reported here achieves better functionality (shutter replacing rolling shutter, 2X frame rate, less column f.p.n., less electronic noise) with different circuits.

A simplified schematic of one column including the pixel, the column amplifier, and the ADC is drawn in Fig.1.

The conventional 5T shutter pixel based on a regular (non-pinned) photodiode can not have good dark uniformity because the switches resetting the photodiode and the pixel memory have statistically different feedthrough. The responsivity of the pixel is reduced to approximately a half of the photodiode responsivity because of the charge sharing between the photodiode and the pixel memory.

These disadvantages were addressed when designing a T-shape 5T shutter pixel which has a common reset switch for the photodiode and the memory, the solution that removes some of the fixed pattern noise. Responsivity was also improved almost twice because the pixel topology allows charge transfer rather than charge sharing. Implemented pixel was based on a traditional photodiode, so we observed some small-signal nonlinearity even when using flushing of the pixel. The non-linearity comes from the tail of the subthreshold current during the charge transfer through the transfer gate. An incomplete transfer should also give rise to the photodiode kTC noise. Implementing the photodiode as a pinned photodiode would improve the pixel linearity and should also remove this component of kTC noise.

The column ADC implemented in the chip is of the successive-approximation type [2], same as of the prototype sensor [1], however it is built of different components. Instead of an offset-reduction calibration DAC in each column, the new ADC extensively uses auto-zeroing. To achieve both good f.p.n. suppression and short decision time (e.g. 10 ns), the autozeroing comparator is made of a 3-stage offset-canceling pre-amplifier (similar to the one from reference [3]) and the reconfigurable dynamic latch which also uses an auto-zeroing for its offset reduction while in reset state. As a result, column f.p.n. was removed to the level non-detectable in the measurements. Instead, we started observing column f.p.n. from the source we did not expect before. The f.p.n. came from the ADC offset circuit generating the offset in each column with small area capacitor. The more bias is applied to the capacitor the more the offset is, and the more is the nonuniformity of the offset.

During the ADC operation, the data is stored in column ADC registers. To increase the readout data rate from the registers, we split the readout into 4-quadrants (Fig.2.). Register bit lines and the data lines were

thereby shortened by the factor of 2 and this was one of the techniques to increase the throughput from the chip twice compared to the prototype chip. To avoid clock skew issues driving the controls to the ADCs and the registers from both left and right, the clock is applied separately to the bottom and the top of the chip to I/O pads which are in the center of the top I/O pad frame and the bottom one, respectively.

We implemented several techniques in the sensor to carry out the experiments on electronic noise reduction.

A pseudo differential pixel readout was the first technique. Our column amplifier was built as a fully differential one while the pixel remained essentially single-ended. To verify pseudo-fully-differential pixel readout, an auxiliary circuit generated a copy of the ground noise with no signal. This copy was fed into the reference input of the column amplifier with the timing identical to the pixel readout. Two different noise reference generation solutions were tried with approximately same result.

The second technique was in reducing transient currents in digital circuits of the column ADCs. Instead of typically used SRAM cells we used DRAM cells to store the data and to control the status of the ADC conversion capacitors.

The third technique to reduce electronic noises was the supplying of the substrate of the ADC digital circuits with analog ground.

The combination of the three techniques gave a good overall result. The electronic noise which typically shows as a row-wise noise, did not come up, whereas it was a big issue in the sensors we developed using the previous sensor technology [1]. It remains unclear which technique contributed into the noise reduction the most.

There also was one negative outcome from the ground noise experiment- a worsening of the yield of the column ADCs, somewhat we never experienced before with the previous ADC topology. The yield loss was proven to be attributed to the leakage from some column DRAM cells, facilitated with the digital ground bounces. In average, one ADC in a thousand was failing. When running corner lots, the yield has been higher for slow-slow transistor models. With little redesign of DRAM cells this yield issue can be completely solved with no impact on the achieved substrate noise rejection.

The results of the sensor characterization are summarized in Table 1, and Fig.4 presents a minimally color-corrected JPEG-compressed image from the sensor.

References

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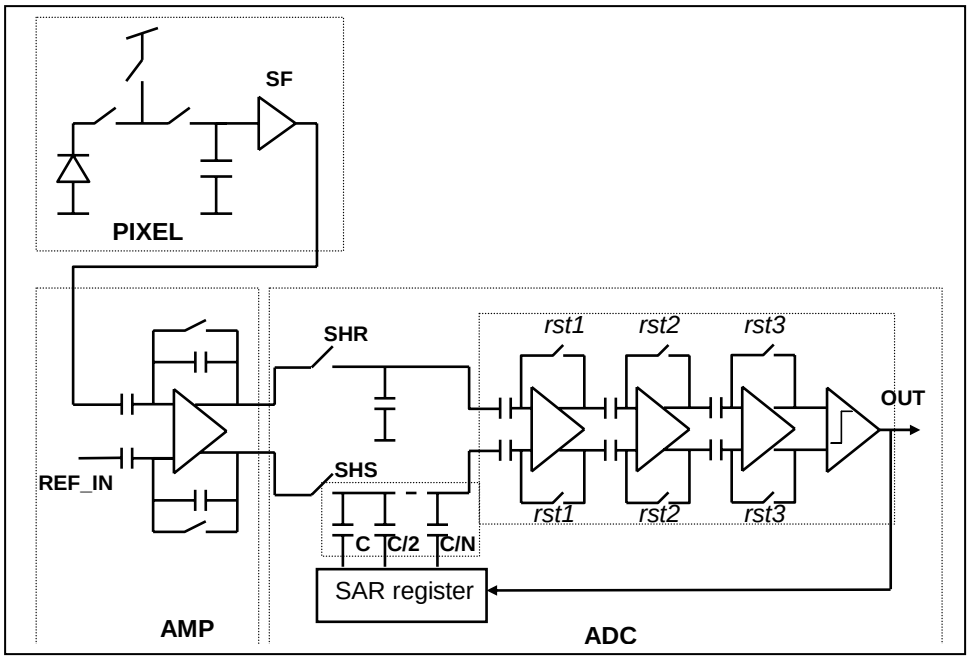

Fig.1. Pixel and column readout simplified schematic

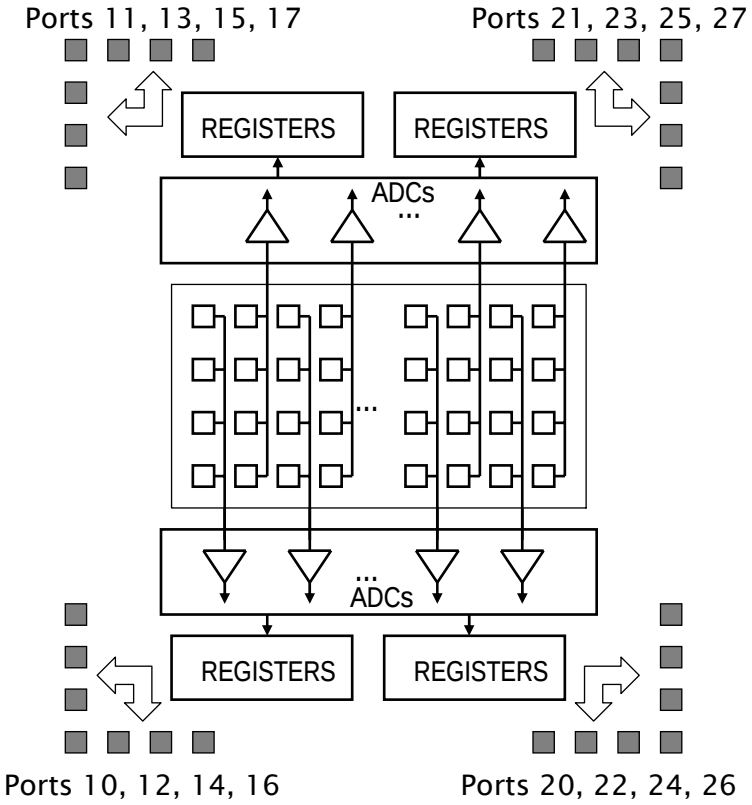

Fig.2. Readout architecture of the 4 Mpixel sensor

Fig.3. A sample picture taken with the 4 Mpixel sensor, with minimum color correction

Table 1

Process	0.25um 1P4M
Array size	4.1Mpix, 2368x1728
Pixel	7um 5T shutter, T-type
Output	16 ports x 10 bit
Max clock rate	120 MHz
Max frame rate	440 Fps @ full resolution
Power	<1.5W
Full well/ noise	25,000e-/30e-
Responsivity	4V/Lux*s @550nm
DSNU	150e- rms