Analysis of Source Follower Random Telegraph Signal Using nMOS and pMOS Array TEG

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***Abstract* - In this work, Random Telegraph Signal (RTS) in source follower circuits is studied using an advanced TEG including dependency on MOSFETs carrier type, gate size and operation bias conditions. Appearance probabilities and noise intensities of RTS for pMOSFETs are shown to be less problematic than these of nMOSFETs for various gate sizes and bias conditions.**

I. INTRODUCTION

It has been recently recognized that Random Telegraph Signal (RTS) noise occurs in source follower circuits in pixel is one of the most crucial contributor to the image quality degradation of deep sub-micron CMOS image sensors because it is difficult to be eliminated by noise reduction circuitry [1-2]. It has been reported that the RTS amplitudes become more significant as MOSFETs' gate size are scaled down [3-4]. Then, understanding of the physical origin of RTS and its suppression are of the urgent tasks for the further increase of image sensor performances, such as higher density, higher speed and wider dynamic range. To understand RTS occurrence mechanism, statistical analysis of RTS is indispensable. However, there is no efficient evaluation method of RTS until now. Then, this work employs an advanced Test Element Group (TEG) for evaluation of both nMOSFETs and pMOSFETs with total number of over 10^6 MOSFETs to statistically analyze RTS. Dependence of appearance probabilities of RTS in enormous number of MOSFETs on carrier type, gate size, gate overdrive voltage and substrate bias conditions are extensively studied using the TEG. And then, RTS parameters such as amplitude, mean time to capture ($<\tau_c>$) and mean time to emission ($<\tau_e>$) can be analyzed in a short time.

II. TEG STRUCTURE AND EVALUATION SYSTEM

Fig. 1 shows circuit schematic of the TEG for nMOSFETs (a), pMOSFETs (b) and the picture image of TEG (c), respectively. Bias voltages V_{DD} and V_G are applied to all the measured MOSFETs simultaneously. The operating point of the measured MOSFETs can be controlled by the values of V_G and I_{DS}, where I_{DS} is the drain current of the current source transistors placed in every column and that is tunable by the value of V_{ref}. As shown in Fig. 1 (d), electrical characteristics of each MOSFET in the source follower circuit is obtained as V_{gs}, which is given by an output voltage V_{out} and a setting V_G under a constant I_{DS}. A large number of MOSFETs' characteristics can be measured in a very short time by scanning the values of V_{out} from each cell using the horizontal and vertical shift resistors. Variation of stationary electrical characteristics in the MOSFETs is observed from variation of time mean values of V_{gs}. Figs. 2 (a) and (b) show the result of the stationary V_{gs} variation under constant I_{DS} = 1μA, which can be assumed threshold voltage variation of MOSFETs included in the array TEG [5]. Random noise within a MOSFET is obtained by measurement of transition of V_{gs} in time-scale. A typical result of RTS is shown in Fig. 3. In this system, since I_{DS} is kept constant during a measurement, random noise in a MOSFET would account for the random signals in V_{gs}. Thus, higher and lower V_{gs} states that are indicated in Fig. 3 correspond to the captured and emission states, respectively. It is because that when a conduction carrier is trapped, a higher gate overdrive voltage is needed for a MOSFET to keep the drain current constant since the inversion layer carrier mobility is degraded as well as the number of the carriers becomes smaller due to the trapped carrier. Several gate sizes of both n- and pMOSFETs are included in the designed TEG that is summarized in Table 1, and manufactured by a 0.18 μm, 1 Poly 2 Metal standard CMOS technology.

III. RESULTS AND DISCUSSIONS

Fig. 4 (a) shows the distribution of the standard deviations of the V_{gs} fluctuation for one MOSFET in time-scale (σ_R) obtained by measuring the continuous 300 outputs of each MOSFET of which sampling rate is 0.7 sec/cell. Fig. 4 (b) shows the time-domain V_{gs} behaviors of nMOSFETs at various σ_R points. In an image sensor system, RTS is more problematic when its amplitude (*A*)

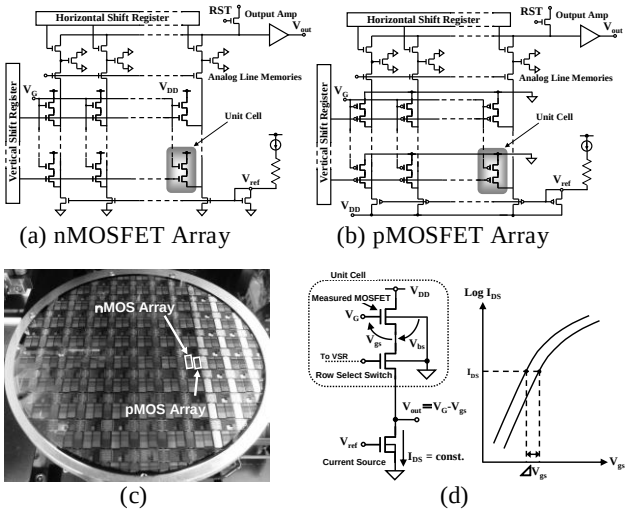
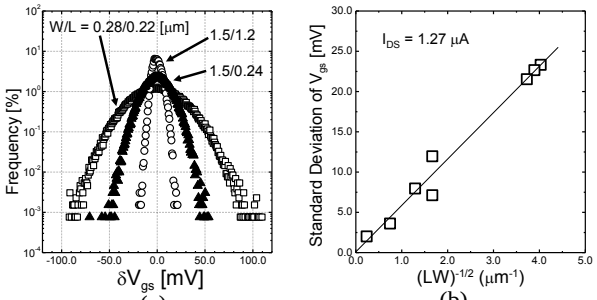


Fig. 1 (a), (b) Circuit schematics for n- and pMOSFET arrays, (c) picture image of TEG in a wafer and (d) method to measure electrical characteristics of MOSFET in the source follower circuits.

Table 1 Gate sizes and the number of MOSFETs manufactured in the n- and pMOSFET array TEG

Gate Length (μm)	0.22	0.22	0.24	0.24	0.4	1.2	1.2	1.2	
Gate Width (μm)	0.28	0.3	0.3	1.5	1.5	0.3	1.5	15	total
No. of nMOSFETs	131,072	131,072	131,072	131,072	131,072	65,536	65,536	16,384	802,816
No. of pMOSFETs	81,920	81,920	81,920	81,920	81,920	40,960	40,960	10,240	501,760



(a) (b)

Fig. 2 (a) Distribution of stationary δV_{gs} which is difference value between V_{gs} of each MOSFET and the mean value of V_{gs} under constant I_{DS} = 1μA with various gate sizes for nMOSFETs and (b) dependence of the standard deviation of stationary V_{gs} variation on gate sizes.

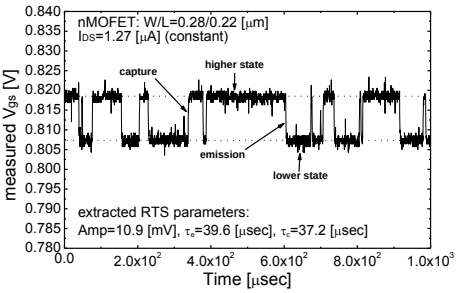
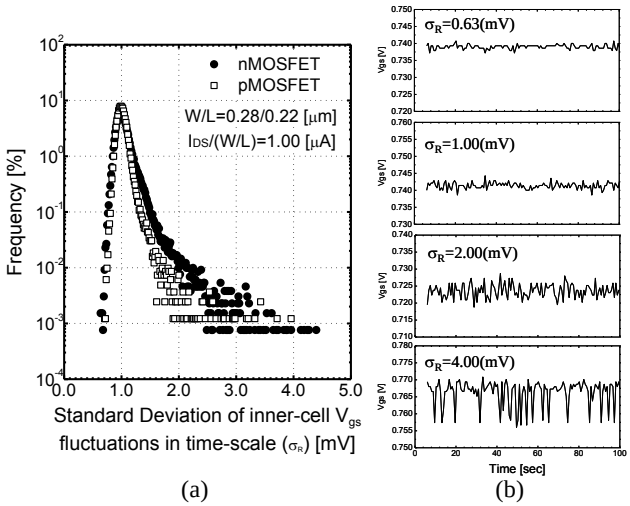


Fig. 3 V_{gs} behavior of a nMOSFET in time-scale. Constant I_{DS} of 1.27 [μA] is applied during the measurement. Signal transitions due to trapping and emission of a conduction carrier are indicated.



(a) (b)

Fig. 4 (a) Distribution of the standard deviation of V_{gs} fluctuation for one MOSFET in time-scale of n- and pMOSFETs with W/L=0.28/0.22 [mm] and (b) time-domain V_{gs} behaviors of nMOSFETs with various σ_R when sampling rate = 0.7 sec/cell.

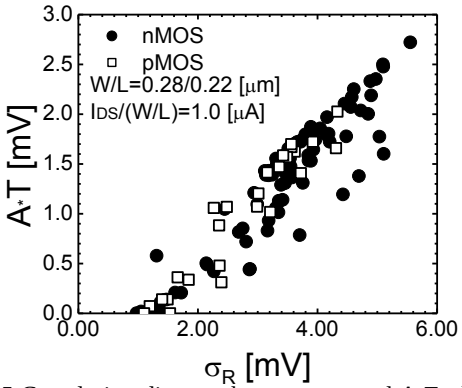


Fig. 5 Correlation diagram between σ_R and A_*T when sampling rate = 0.33 μsec/cell. A strong correlation is observed.

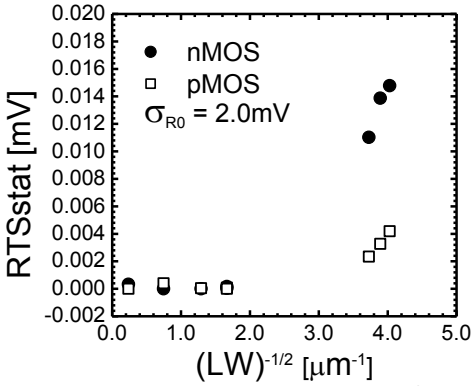


Fig. 6 RTS statistical indicator: *RTSstat* as functions of gate size for nMOSFETs and pMOSFETs for σ_{R0} = 2.0 [mV]. Results clearly show that pMOSFETs has smaller *RTSstat* than nMOSFETs.

become higher [6]. Here, signal transition probability is given by the following equation [7].

$$T = \frac{< \tau_e >< \tau_c >}{(< \tau_e > + < \tau_c >)^2} \qquad (1)$$

where $<\tau_e>$ and $<\tau_c>$ are mean value of time-to-emission and time-to-capture for the trap to generate RTS, respectively. Then, A_*T is defined as a factor to characterize RTS noise intensity of a MOSFET. To examine the correlation between σ_R and A_*T, we measured various MOSFETs and extracted A and T each MOSFET. Fig. 5 shows the correlation between σ_R and A_*T. It is obviously shown that σ_R and A_*T have a strong correlation. Then, following parameter is defined as a statistical factor to evaluate RTS among MOSFETs with various gate sizes or bias points.

$$RTSstat = \sum_{\sigma_R=\sigma_{R0}}^{\infty} \sigma_R \cdot freq(\sigma_R) \qquad (2)$$

where σ_{R0} is a minimum value of the range of σ_R to be analyzed and $freq(\sigma_R)$ is the appearance probability corresponding to each σ_R. Fig. 6 shows the extracted *RTSstat* from the σ_R measurement results as functions of the gate size for n- and pMOSFETs. The results clearly show that *RTSstat* increases as gate size is scaled down. Moreover, pMOSFETs have smaller *RTSstat* than that of nMOSFETs for various gate sizes indicating that RTS is more problematic in nMOSFETs than pMOSFETs.

Fig. 7 shows the correlation between A^*T and stationary V_{gs} of each nMOSFET at $I_{DS}/(W/L) = 1\mu A$. The results show that the correlation is very small indicating that the origins of the RTS and stationary V_{gs} variation are not same.

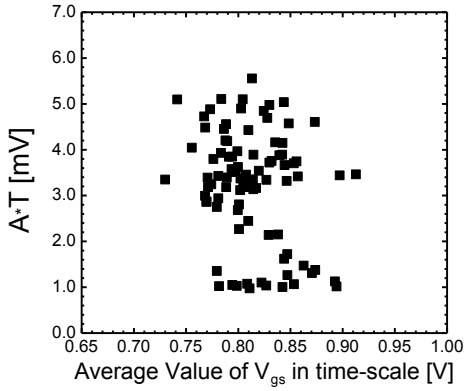


Fig. 7 Correlation between A^*T and stationary V_{gs} of each nMOSFET with W/L = 0.28/0.22 [μm]. The correlation is confirmed to be very small.

In addition to the gate size, RTS characteristics are analyzed for various bias conditions. Figs. 8 (a-e) show the RTS results of a nMOSFET and a pMOSFET at various I_{DS} and a fixed $|V_{bs}| = 1.0$ V. Figs. 9 (a) and (b) show the $<\tau_e>$, $<\tau_c>$ and RTS amplitudes as a function of I_{DS} for the n- and the pMOSFET with W/L = 0.28/0.22 μm. Figs. 10 (a) and (b) show Gumbel distributions in terms of σ_R for various I_{DS} for n- and pMOSFETs and Fig. 10 (c) shows *RTSstat* as a function of I_{DS}, respectively. The results show that as gate overdrive voltage increases, $<\tau_e>$ increases, $<\tau_c>$ decreases, the RTS amplitude decreases and RTS appearance probability of large σ_R cells decreases. Thus, *RTSstat* decreases as gate overdrive voltage increases as Fig. 10 (c) shows. Moreover, *RTSstat* of pMOSFETs are smaller than nMOSFETs in all the measured I_{DS}.

Figs. 11 (a-e) show the RTS results of a nMOSFET and a pMOSFET at various $|V_{bs}|$ and a fixed $I_{DS}/(W/L)$ = 1 μA. Figs. 12 (a) and (b) show the $<\tau_e>$, $<\tau_c>$ and RTS amplitudes as a function of $|V_{bs}|$, Figs 13 (a) and (b) show Gumbel distributions in terms of σ_R for various $|V_{bs}|$ for n- and pMOSFETs and (e) shows *RTSstat* as a function of $|V_{bs}|$. The results show that as $|V_{bs}|$ increases, for the nMOSFET, $<\tau_c>$ decreases, $<\tau_e>$ increases and *T*

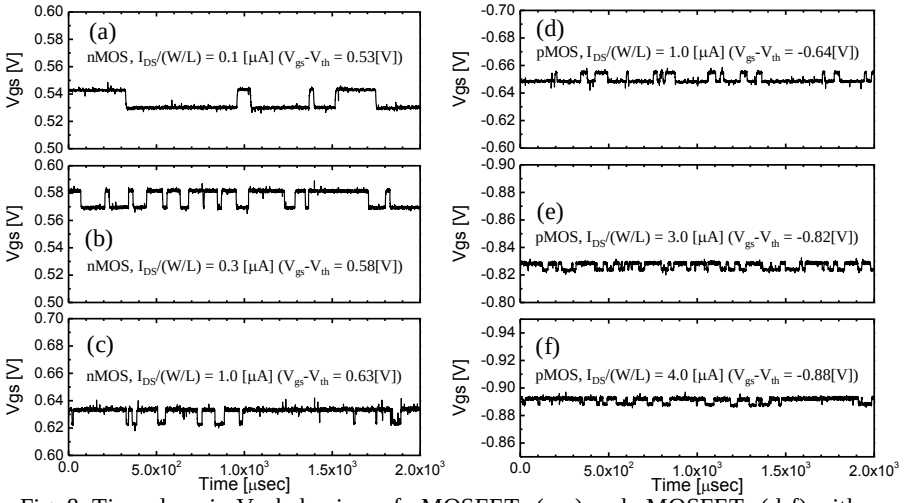


Fig. 8 Time-domain V_{gs} behaviors of nMOSFETs (a-c) and pMOSFETs (d-f) with gate size of W/L=0.28/0.22 [μm] for various I_{DS}, respectively. $|V_{bs}|$ during the measurements is 1.0 [V]. The results show that amplitudes of RTS decreases as I_{DS} increases. Also, probability of higher state (captured state) increased as I_{DS} increases.

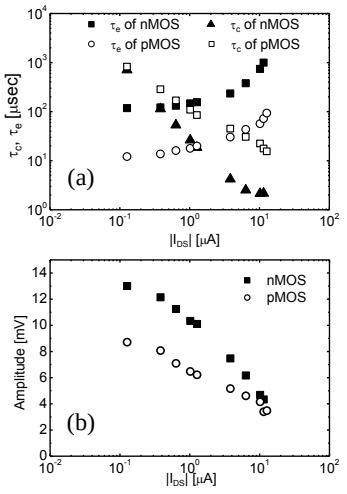


Fig. 9 (a) Capture and emission time constant, (b) RTS amplitude as function of gate overdrive voltage, respectively.

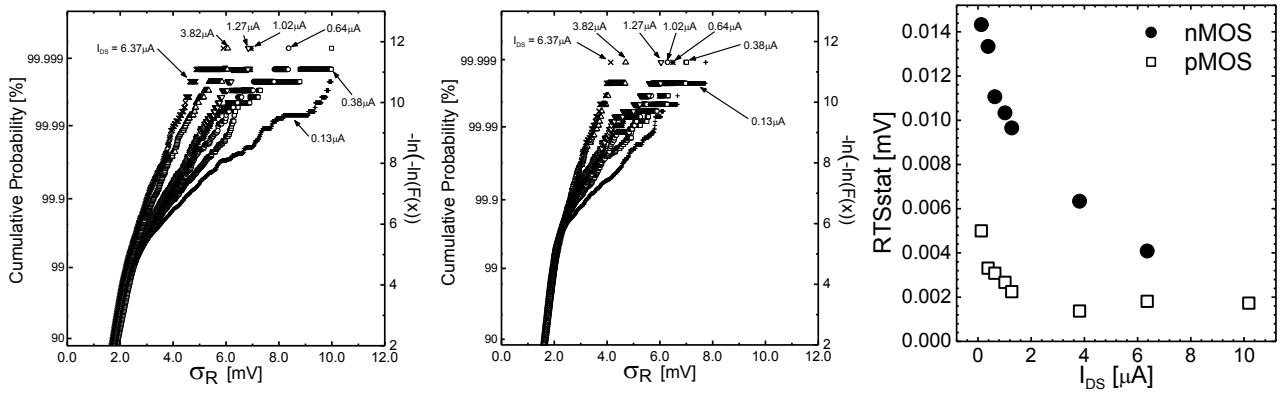


Fig. 10 (a) Gumbel distributions of the σ_R for nMOSFETs, (b) pMOSFETs and (c) shows the *RTSstat* as function of I_{DS} for n- and pMOSFETs.

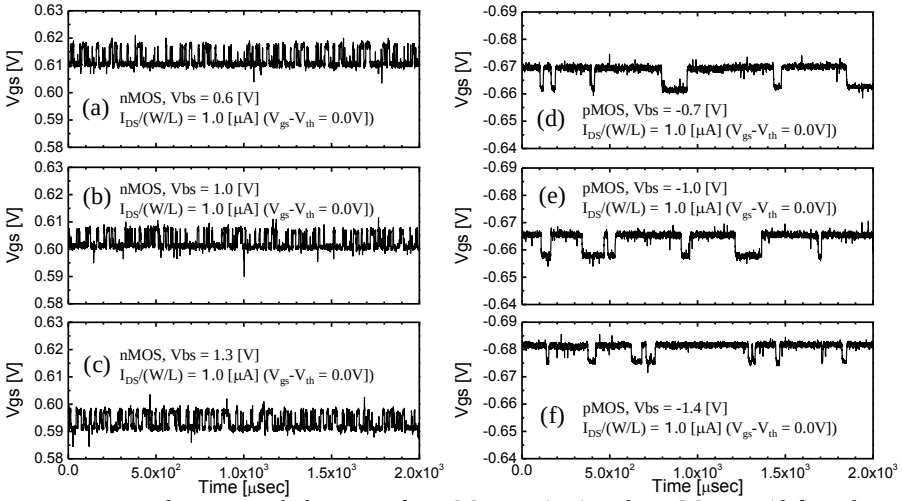


Fig. 11 Time-domain V_{gs} behaviors of nMOSFETs (a-c) and pMOSFETs (d-f) with the gate size of W/L = 0.28/0.22 [μm] for various $|V_{bs}|$, respectively, where I_{DS} during the measurements is 1.0 [μA] (at threshold voltage).

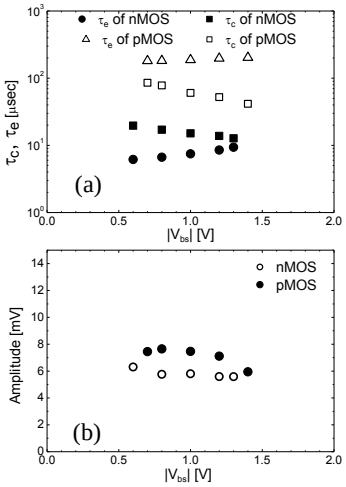


Fig. 12 (a) Capture and emission time constant and (b) RTS amplitude as functions of back substrate voltage(V_{bs}).

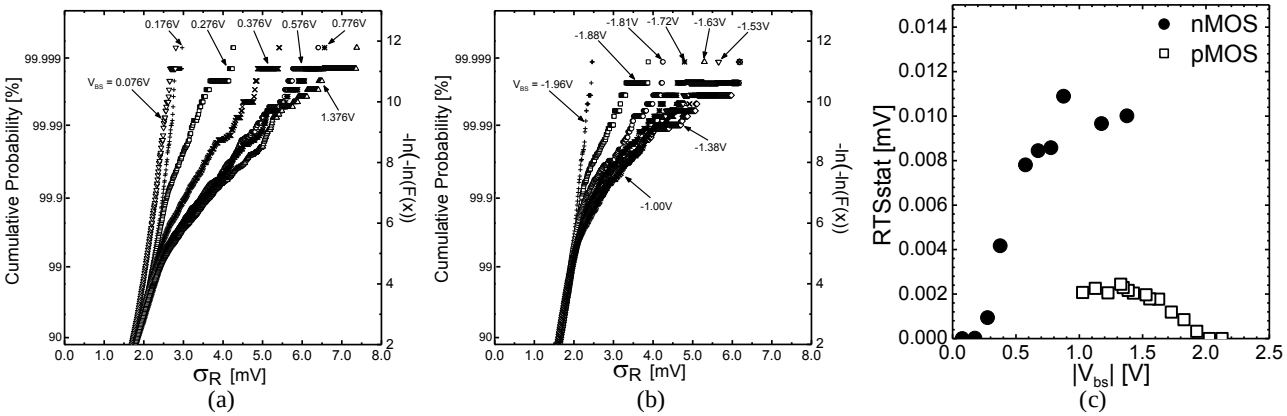


Fig. 13 (a) Gumbel distributions of the σ_R for nMOSFETs, (b) pMOSFETs and (c) shows the *RTSstat* as a function of $|V_{bs}|$ for n- and pMOSFETs.

increases. Also, as $|V_{bs}|$ increases, the RTS amplitude does not change much and RTS appearance probability of large σ_R cells increases. On the other hand, as $|V_{bs}|$ increases for the pMOSFET, $<\tau_e>$ increases, $<\tau_c>$ decreases and then *T* decreases. Also, as $|V_{bs}|$ increases, the RTS amplitude does not change much and RTS appearance probability decreases for pMOSFETs. Consequently *RTSstat* increases for nMOSFETs and decreases for pMOSFETs as $|V_{bs}|$ increases as Fig. 13(c) shows. Moreover, *RTSstat* of pMOSFETs are smaller than that of nMOSFETs in all the measured $|V_{bs}|$. These tendencies would indicate that energy level distributions of traps contributing to RTS are different for electrons and holes.

IV. Conclusion

In this work, Random Telegraph Signal in source follower circuits is statistically evaluated using the newly developed array TEG for characterizing nMOSFETs and pMOSFETs. The results obtained from more than 10^6 sample cells revealed the following four key findings.

1. RTS is severer in nMOSFET than in pMOSFET.
2. *RTSstat* increases as transistor gate size becomes smaller.
3. RTS appearance probability, RTS amplitude and *RTSstat* decrease as applied gate overdrive voltage increases for both nMOSFETs and pMOSFETs.
4. *RTSstat* increases for nMOSFETs and decrease for pMOSFETs as applied substrate voltage increases.

Findings obtained using the developed array TEG would give very useful information to the circuit design of highly noise tolerant image sensors. Moreover, statistical RTS measurement using the TEG would give an efficient evaluation of LSI manufacturing processes.

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References

[1] J. Y. Kim et al., *IEEE Workshop on CCDs & AIS*, p.142, 2005.
[2] X. Wang et al., *IEDM Tech. Dig.*, p.115, 2006.
[3] A. Asenov et al., *IEEE Trans-ED*, **50**, 3, p.839, 2003.
[4] N. Tega et al., *IEDM Tech. Dig.*, p.491, 2006.
[5] S. Watabe et al., *JJAP.*, **46**, 4B, p.2054, 2007.
[6] C. Leyris et al., *Proc. 32nd ESSCIRC*, p,376, 2006.
[7] K. S. Ralls et al., *Phys. Rev. Lett.*, **52**, 3, p.228, 1984.