Continuous Time Column Parallel Readout for CMOS Image Sensor

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INTRODUCTION

As advances continue in process technology with features shrinking it is increasingly common for CMOS image sensors to contain pixels with dimensions below 2μm square. As the pixel size reduces, similarly the light sensitive area is reduced. Although this has been compensated for,to a degree, by an increase in the conversion gain, a reduction in the number of incident photons means the voltage swing for a given illumination has decreased. In a standard active pixel sensor architecture the pixel voltage is buffered via a source follower to the column bitline where it is sampled and converted to a digital word. Noise from the source follower, sampling and ADC all contribute to the total noise in the image.

Regardless of the process or design, a sampled system will be subject to kTC noise. If the signal swing from the pixel reduces for a given illuminatiion level, the sampling capacitor would need to increase by the square of the reduction to maintain the same SNR. A method of reducing the impact of kTC noise (and noise in subsequent stages) is to add an amplification stage into the column[1]. The design of such an amplification stage is obviously crucial so as not to introduce further noise but will unavoidably require extra silicon area.

This paper presents a column readout that operates without any sample and hold structure with an aim to reduce the readout noise whilst consuming a minimum of silicon area. The continuous time architecture has been fabricated as the readout for a 5Mpix CMOS image sensor and targetted towards a 12bit ADC resolution. The imaging array shares devices to give an effective 1.75 transistors per pixel[2] where the pixel size is 1.75μm in a 90nm minimum feature size technology.

Sensor and column architecture

The schematic of a single column with connected pixel is shown in Figure 1 where the capacitors are realised by metal-metal structures to achieve good linearity and matching. At the end of the set exposure period the RESET control signal to the pixel will fall to leave the ‘black’ or ‘reset’ level of the pixel on the floating diffusion node(FDN). This voltage is buffered by the pixel source follower to the column. During this time both amplifiers 1 and 2 in the column are held in their auto-zero state and the ramp is grounded. When the reset level of the pixel has settled in the column the AZ1 switch will first open causing charge injection onto the input node of the amplifier. By careful sizing of the AZ1 switch, input capacitors and amplifier gain, the output of the first amplifier can remain unsaturated allowing the input offset to be stored in capacitor C3.

After AZ2 has fallen the transfer gate in the pixel can be pulsed to transfer the light generated charge to the floating diffusion thus causing a similar drop in the column voltage and a reduced drop at the input of the first amplifier. When the column voltage has settled the DAC can be enabled to generate the RAMP which is applied to input capacitor CIN2. The capacitively coupled ramp will cause the input of the first amplifier to rise and at some point the output will flip. This flip will be cascaded through to the 2nd and third amplifiers and controls when the SRAM stores the count value. The READ signal to the addressed row will remain on for the duration of the ADC conversion[3] thus requiring the floating diffusion to maintain the light generated charge.

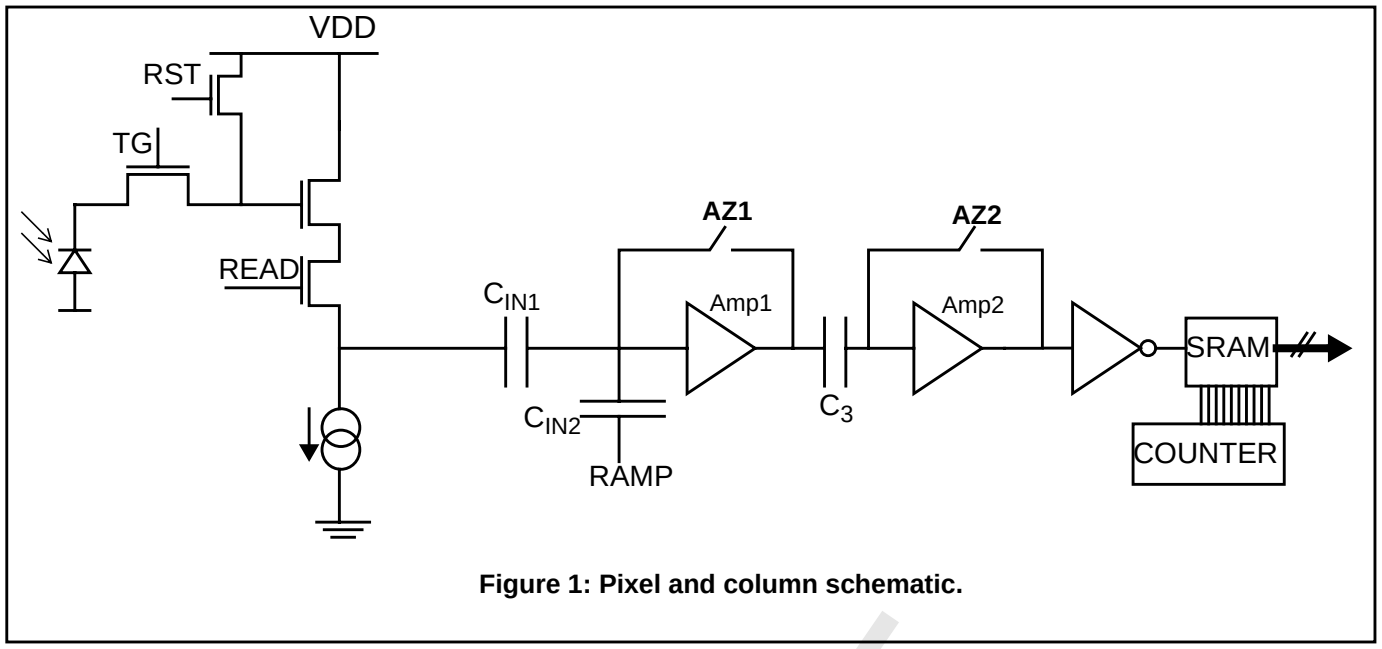


Figure 1: Pixel and column schematic.

The chip is composed of an array of 2640x1992 pixels arranged to share devices to give an effectice 1.75 transistors per pixel. Rows of pixels are addressed by a Y-decoder situated to the right of the imaging array and readout through top and bottom column parallel ADC's and SRAM. The SRAM output from the top and bottom are routed to the mid left of the chip and recombined before the parallel data is connected to pads. The power management circuitry including bandgap, charge pumps and DAC is situated to the right of the Y-Decoder. A ring oscillator is also included on chip to generate a high speed count which is sent to the SRAM and used to control the DAC. A chip plot is shown in Figure 5.

Readout of the imaging array is done with a rolling shutter type exposure. Opearting at a pixel clock of 80MHz allows 15fps and permits 33us to reset, read and convert addressed rows. At this data rate a DAC frequency of around 200MHz is required to achieve a true 12-bit conversion for the single slope ADC. Non-linear ramp schemes that exploit the characteristics of photon-shot noise to reduce the conversion time have been proposed[4][5]. However, a linear 12-bit conversion has been realised to maintain effective colour processing[6]. The ring oscillator was made programmable from 80MHz to just under 300MHz and the noise at different frequencies is shown in the measurements section.

Measurements

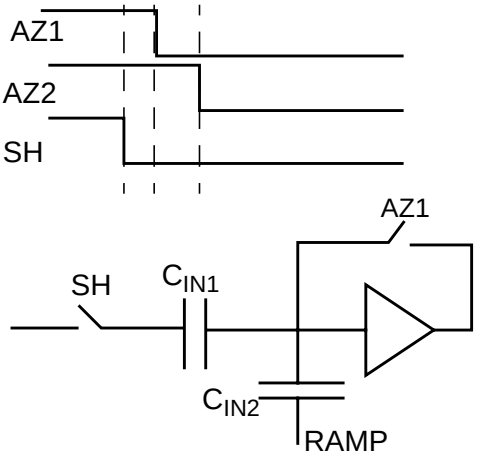


Figure 2: Schematic and timing to measure ADC noise.

The temporal noise contribution of different sections of circuitry in the readout chain was measured by applying different timing modes. To measure only the ADC noise it was necessary to add a sample and hold switch in series with C_{IN1} of the comparator. By sampling the 'reset' level of the pixel before AZ1 falls, the noise of the preceeding circuitry can be removed, leaving only ADC noise. It should be noted that the ADC conversion (mV/code) is different for sampled and continuous time operating modes.

The noise is plotted in Figure 3 for different DAC/SRAM speeds. The readout speed from the device was fixed at 48MHz to give approx. 9 frames per second. The Source follower noise was calculated from

$V_{NSF} = \sqrt{(V^2_{NTOT} - V^2_{NADC})}$ where V_{NTOT} is the total noise and V_{NADC} is the ADC noise.

It can be seen that the ADC temporal noise shows a gradual increase with the ADC/SRAM operating frequency. However a slight increase in the SF noise must also occur to account for the total noise. A thermal change may account for this increase.

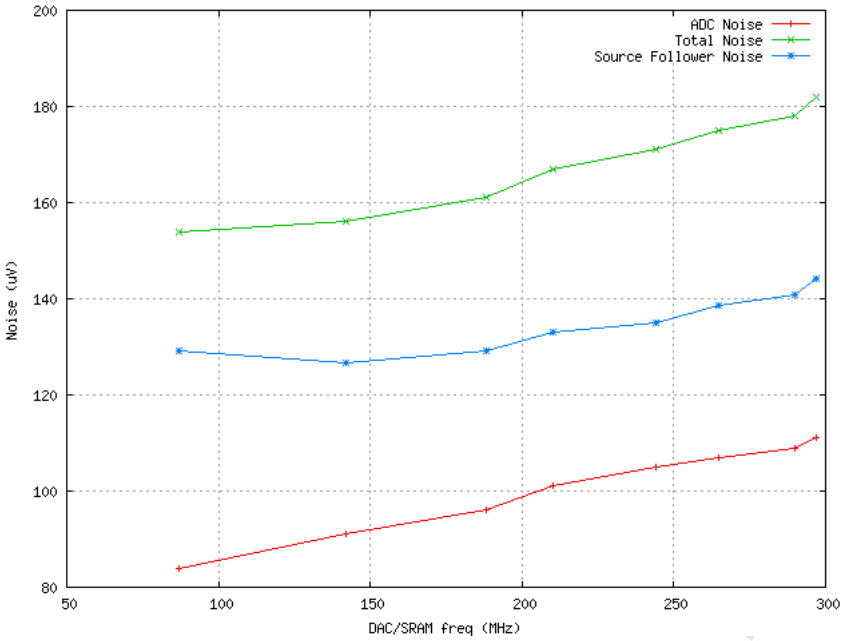
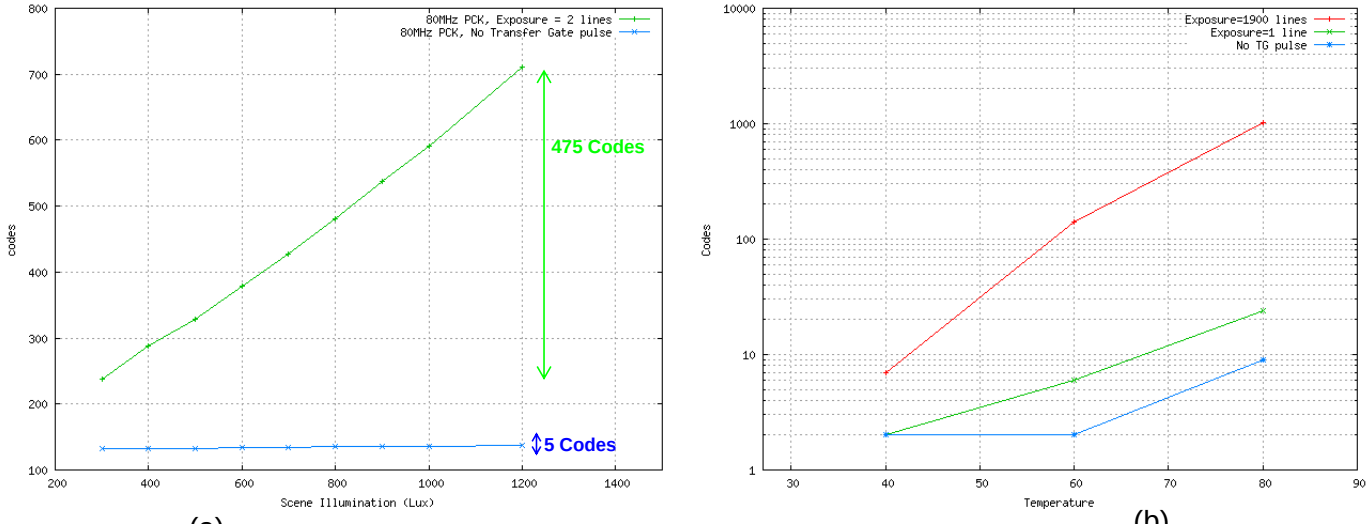


Figure 3: Plot of temporal noise v's Conversion speed.

An important consideration of the continuous time readout is how well charge is stored on the floating diffusion node. Since the voltage needs to be held for the duration of the ADC conversion it is important it is not degraded or corrupted. Illumination and temperature are two important parameters to consider. Since the floating diffusion is located in the pixel array it will be subject to the incident illumination. Microlens' if used will help direct light away from the FDN, however, in the same way that dark current increases with temperature, the leakage on the FDN will do likewise. The leakage is measured by disabling the transfer gate pulse. The plots of Figure 4 provide additional curves without the transfer gate disabled so that the leakage can be compared to the signal generated by the photodiode. The measurements were taken with a reduced ramp range so that one code is less than 8uV.



(a) (b)

Figure 4: Plot of leakage on FDN (a) with scene illumination (80MHz PCK, image average) (b) with temperature(48MHz PCK, per pixel difference with image at 27deg).

Figure 4(a) compares an image with exposure of 2 lines with an image where the transfer gate is disabled. This worst case test condition shows the signal is still dominant over the leakage. Figure 4(b) provides the same comparison against temperature and shows the FDN leakage to have a much reduced effect compared to the dark current of the pixel.

Conclusion

We have presented a low noise readout architecture for a CMOS image sensor by removing the noise generated in a sampled system. The simplicity of the continuous time architecture allows for a compact layout of the column parallel readout. A full 12-bit linear slope for the ADC is achieved with a high speed DAC and SRAM.

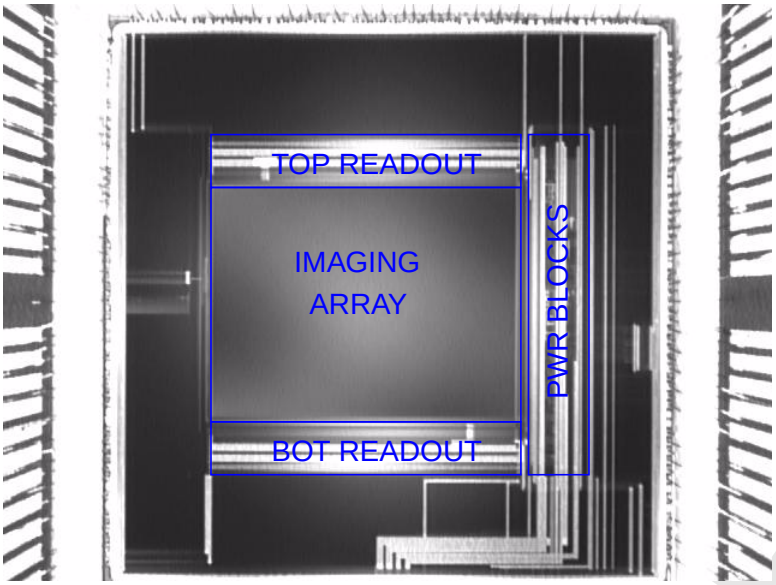


Figure 5: Test chip plot.

Parameter	
Pixel pitch	1.75um
Transistors/pixel	1.75
Array dimensions	2640x1992
Conversion gain at column bitline.	70uV/e^-
Full Well	600mV(8500e-)
Temporal Noise (G16) 210MHz DAC/SRAM -Total -SF -ADC	 167uV (2.4e-) 133uv (1.9e-) 101uV (1.4e-)
VFPN	10uV

Table 1: Imager Characteristics

References

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