

A 2.3e- Read Noise 1.3Mpixel CMOS Image Sensor with Per-Column Amplifier

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Low-noise, low-power, area-efficient CMOS imager readout architecture is studied through four 1.3Mpixel test chips using the same pixel array and silicon area. By employing per-column amplifier in front of column sample-and-hold circuitry and utilizing the extended correlated-double-sampling[1,2] principle, a low 2.3e- read noise is achieved, as compared to 4.2e- with conventional serial analog multi-stage readout chain architecture. The gain stages and 10-bit pipelined analog-to-digital converter (ADC) featured the shared-amplifier with short-reset scheme [3] delivered a maximum of 64x analog gain with differential nonlinearity (DNL) +0.3/-0.6 least significant bit (LSB) and integral nonlinearity (INL) +1.2/-0.75 LSB with 50% lower power consumption.

Based on a 1/4-inch optical format 1.3Mpixel CMOS active-pixel digital image sensor with 1280x1024 resolution and 2.8 μ m pixel size, this sensor requires 2.8V nominal pixel power supply, 1.8V nominal logic supply, and 1.7V to 3.6V I/O. The imager includes a low-noise signal readout chain, a 10-bit ADC, an internal phase-locked loop (PLL), and a 10-bit parallel interface to output pixel data at up to 27 megapixels per second (Mp/s). The imager uses a 2.5T cell 2.8 μ m \times 2.8 μ m pixel configured in common element pixel architecture (CEPA) for high fill factor and light sensitivity. It also uses top and bottom multiple channels with analog signal readout at a rate of 13.5Mp/s, which result in 15 frames per second (fps) at full resolution and 30fps at VGA resolution in full field of view (FOV). Operating power consumption of the chip in full resolution at 15fps is less than 65mW. The chip dimensions are 6.25mm \times 5.2mm.

Figure 1 shows the imager architecture. A conventional serial analog readout multi-stage chain is shown in Figure 2. Figure 3 shows low-noise analog readout chain with per-column amplifier. Figure 4 shows shared-opamp scheme for gain stages and 10-bit pipelined ADC. Figure 5 shows a comparison of capture images. Variation configurations and corresponding readout noises are summarized in Table 1.

References:

- [1] Alex Krymski, Nail Khaliullin, Howard Rhodes, "A 2 e- noise 1.3Megapixel CMOS sensor", IEEE Workshop on CCDs and Advanced Image Sensors, 2003.
- [2] Nobuhiro Kawai, Shoji Kawahito, " Noise analysis of high-gain, low-noise column readout circuits for CMOS image sensors," IEEE Trans. Electron Devices, vol. 51, no. 2, pp. 185-194, 2004.
- [3] Taehee Cho, Sandor Barna, Andrew Lever, Kwang-Bo Cho, Chiajen Lee, "Sharing operational amplifier between two stages of pipelined adc and/or two channels of signal processing circuitry," United States Patent (US 7148833), Dec. 2006.

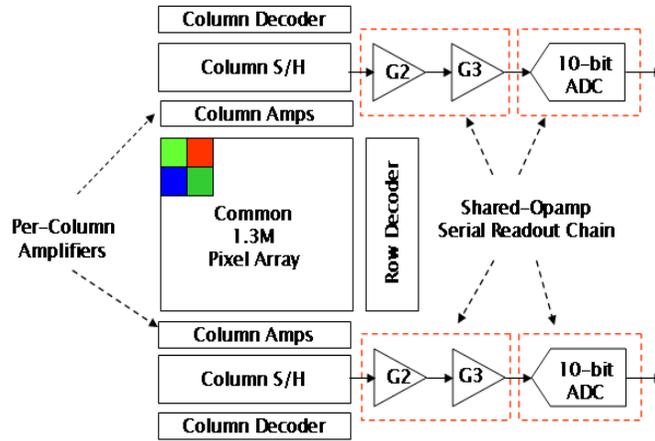


Fig. 1: Overall architecture.

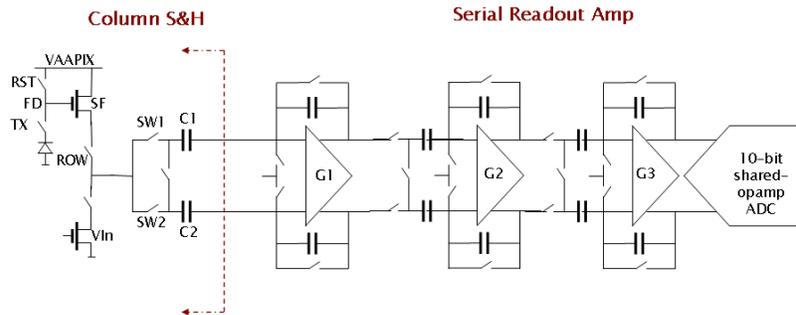


Fig. 2: Conventional serial analog multi-stage readout chain.

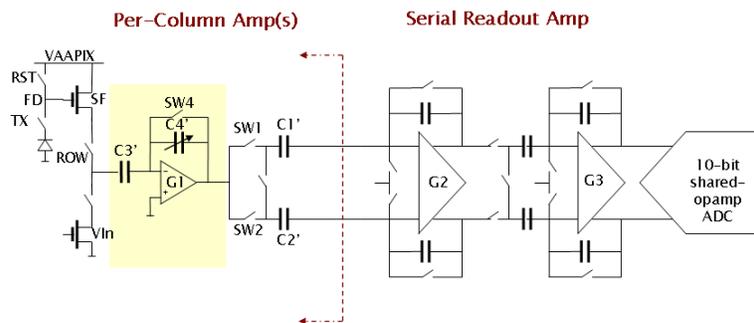


Fig. 3: Analog readout chain with per-column amplifier.

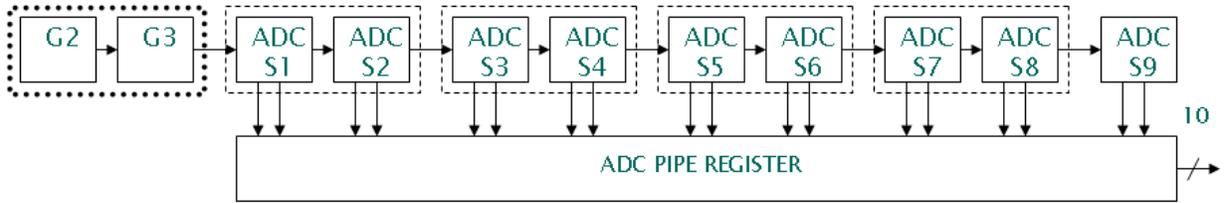


Fig. 4: Shared-opamp scheme for gain stages and 10-bit pipelined ADC.

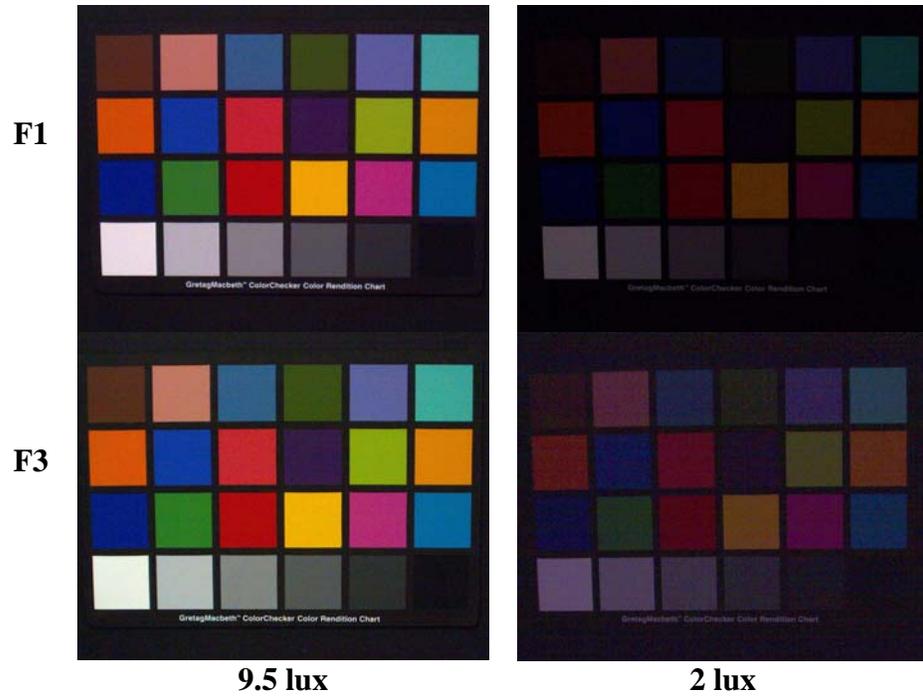


Fig. 5: Comparison of capture images.

Table 1: Variation configurations and corresponding readout noises.

F-CELL	ADC	Per-Column Amp	Spare Amp	G2/G3 shared-opamp	Total gain	Read noise* (e-)
F1	Common 10-bit shared-opmap ADC	Yes	No	Yes	16x	2.82 e-
F2		Yes	Yes	No	16x	2.28 e-
F3		No	Yes	Yes	16x	4.21 e-
F4		Yes	Yes	Yes	64x	2.87 e-

* Measured at 16x total gain