

A High Dynamic Range digital LinLog CMOS image sensor architecture based on Event Readout of pixels and suitable for low voltage operation

Alexandre Guilvard^{1,2}, Pierre Magnan¹, Josep Segura², Philippe Martin-Gonthier¹

¹Supaero, Toulouse, France;

²STMicroelectronics, Crolles, France

¹A. Guilvard, P. Magnan, P. Martin-Gonthier: E-mail : {guilvard, magnan, martingo}@supaero.fr Tel : +33.5.62.17.80.79

²J. Segura : E-mail : josep.segura@st.com Tel : +33.4.76.92.56.94

Several approaches have been developed to extend the dynamic range of image sensor [1] in order to keep all the information content of natural scenes covering a very broad range of illumination. Digital CMOS image sensor are especially well suited to wide dynamic range imaging by implementing dual sampling [2], multiple exposure methods using either column [3] or in pixel ADC [4][5][6], or Address Event Representation [7].

A new architecture of digital high dynamic range CMOS image sensor, suitable for low voltage operation, has been developed that implements a built-in dynamic compression function targeted to LinLog behavior, by combining an event based readout of pixels, the use of multiple integrations per frame (fig.1) and the coding of pixel values using the mantissa-exponent principle [4] [8], to achieve the dynamic range extension.



Fig. 1: Multiple integrations per Frame and output data coding

This architecture is depicted in Fig 2: each pixel implements an ADC based on an autozero comparator and a global voltage ramp (Vramp) generated by a unique 10 bits DAC with a roughly 1,2 mV resolution. In order to have a constant photodiode voltage during digitizing, a snapshot feature has been added to the pixel with a light shielded memory node Csn storing the photodiode voltage that is compared to the ramp value.

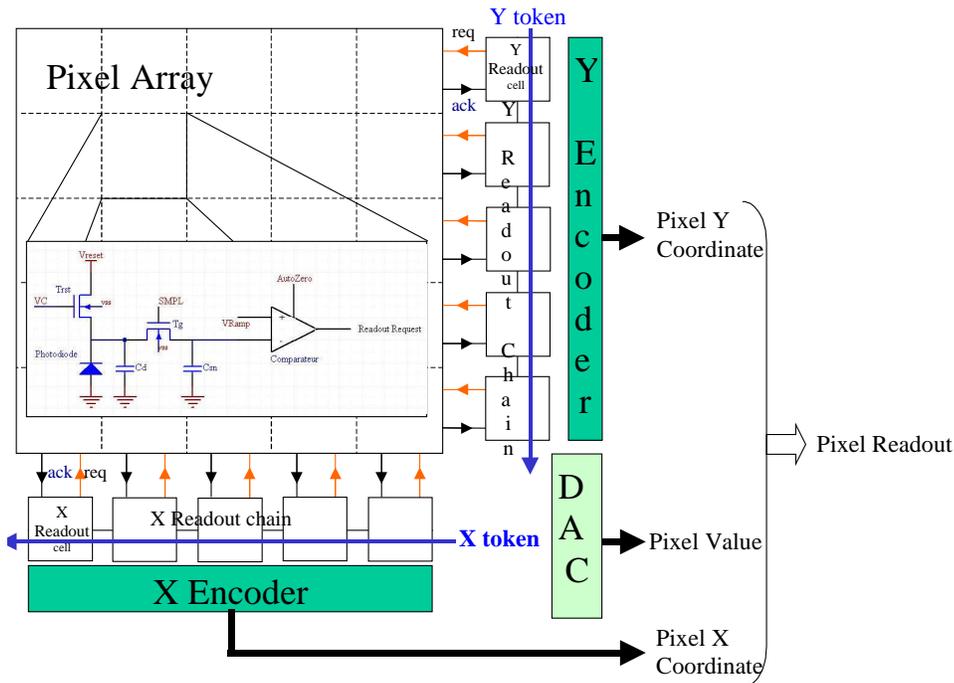


Fig. 2: Pixel and sensor architecture.

The sensor makes use of an innovative and fast event based readout chain to avoid the readout of the entire pixel array after each integration, and so allows a direct capture of the final image from the different exposure times without the need of external reconstruction. After each integration, the ADC ramp rises and for each pixel, when its voltage value is larger than the Csn voltage, the comparator flips, and a readout request is sent by the pixel (reqY). Once detected and processed by the readout chains, the read pixel is attributed the digital input value of the DAC together with its address coordinates. In order to read the array with no pixel loss nor possible conflicts, the readout requests have been splitted into row (Y) and column (X) requests. Two readout chains, one per axis, have been created to allow the circulation of an asynchronous token at very high speed (typically 3 GHz in advanced process, based on the gate propagation delay) as depicted in fig. 3 for the Y axis. For each step of the voltage ramp (VRamp), a scan of all the rows is performed by sending a token on the Y axis. Upon a pixel request, the Y flag is stopped at this line, an acknowledge signal is sent on the row (ackY) by the corresponding readout cell and at the receipt of the acknowledge signal, an in-pixel logic block emits the readout request on the column (reqX). As a requesting line has been detected, the X flag is started to scan the column. The X flag is stopped on the requesting column and an acknowledge signal is send (ackX). At the receipt of the two acknowledge signals, the pixel is attributed the DAC digital input value and is placed in standby mode, the comparator output being disconnected from readout chain (this requires logic blocs in the pixel) until the capture of the next frame. Therefore, each pixel is read only once during a given frame. and their data is externally memorized. Thanks to the request-acknowledge readout principle, no conflicts or loss can occur.

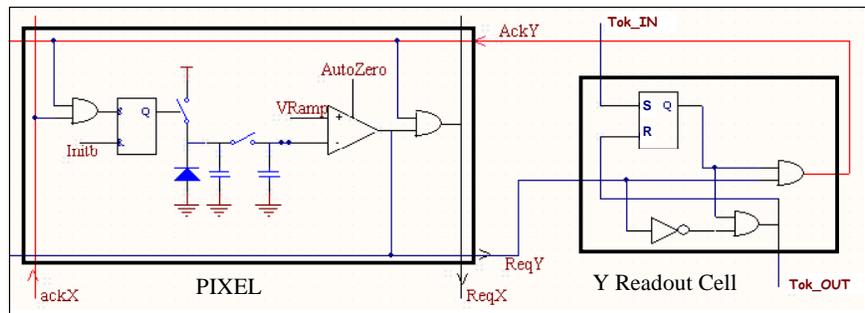


Fig. 3 Pixel and readout cell interaction (simplified view)

Doing so, each possible illuminance level of the scene is processed in a unique integration. The integrations are performed from the shortest to the longest, and only a part of the photodiode voltage swing is explored by the DAC at each integration $[V_{refmin}, V_{refmax}]$ (Fig 4).

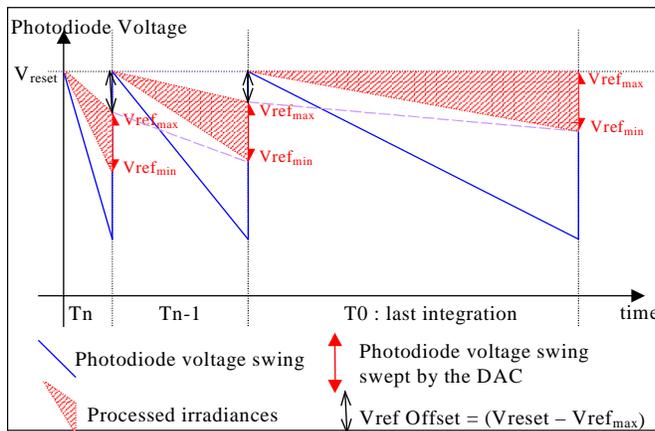


Fig. 4 Distribution of the scene dynamic range to the different integrations

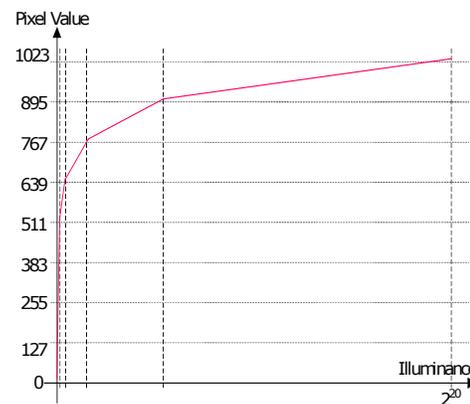
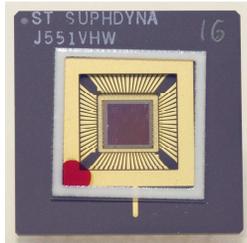


Fig. 5: Segment approximation of LinLog dynamic compression curve obtained with 8 integrations per frame with Tint Ratio = 4

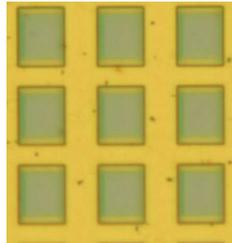
The compression function is build from segments whose slope ratios are defined by the integration times ratios. As an exemple, in fig. 5, 8 integrations with a constant ratio equal to 4 are used to produce a Lin-Log compression characteristics. Ratios between the slope of the segments building the compression function are defined

by the ratios between the integration times This architecture is entirely digital and so well suited for the low voltage supply of advanced processes.

The previous principles have been implemented in a validation prototype (fig.6) - 511x511 pixels array- realized in the STMicroelectronics 0.13 μ m CMOS standard (non imaging) technology with simple oxide 1.2 V transistors; table 1 provides the key features. This sensor operates at video rate and the pixel containing 42 transistors and an Nwell photodiode.



the sensor



view of the pixels

Sensor Prototype target specifications	
Resolution	511 x 511
Pixel size	10 μ m x 10 μ m
Number of transistor per pixel	42
Fill Factor	25 %
Output resolution	10 bits
DAC step	1.17mV
Clock Frequency	50 MHz
Conversion gain @pixel level	40 μ V/e
Power supply	1,2 V
Supported dynamic range	>100dB

Table 1: Sensor Prototype target specifications

Fig. 6: 511x511 pixel array prototype implemented in STMicroelectronics 0.13 μ m digital CMOS technology.

The event-driven readout principle is completely functional and no error in the readout process occur but due to unexpected leakage in the non optimized technology used, still in investigation at the time of paper writing, the linear voltage swing of the pixel is limited to 300mV as shown in fig.7.

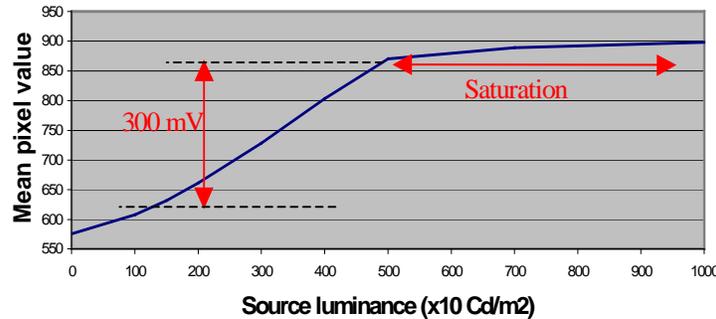


Fig.7: Transfer characteristic in linear mode (@Tint=5ms) demonstrating a limited linear voltage swing of 300mV

Despite this limitation in the swing, the DR extension principle still works but with less versatility in the integration time ratio and so in the produced characteristics. Fig. 8 shows the Transfer Characteristic achieved with a Tint Ratio setting of 3 and demonstrates a significant DR extension (more than 30 dB).

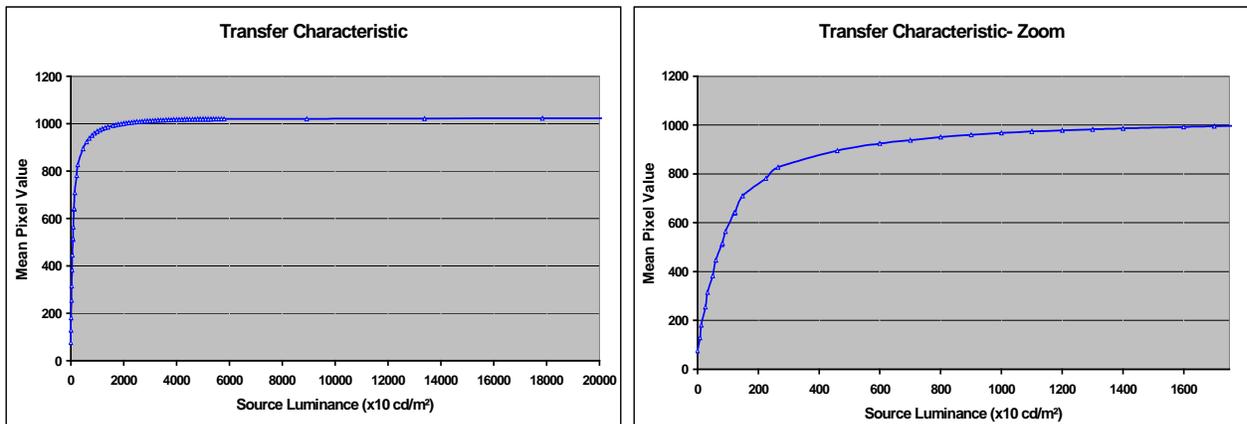


Fig. 8: Measured Transfer characteristic for Tint Ratio setting= 3 (from 3 μ s to 6.5 ms).The source-sensor distance is more than 3 times shortest than for the linear characteristic measurement

Images of HDR scenes have been captured with this sensor (Fig. 9) and the 4 images (splitted 256 gray scale level) demonstrate that all the information of the HDR image is available. This HDR image is rebuilt in memory with no need of post processing.

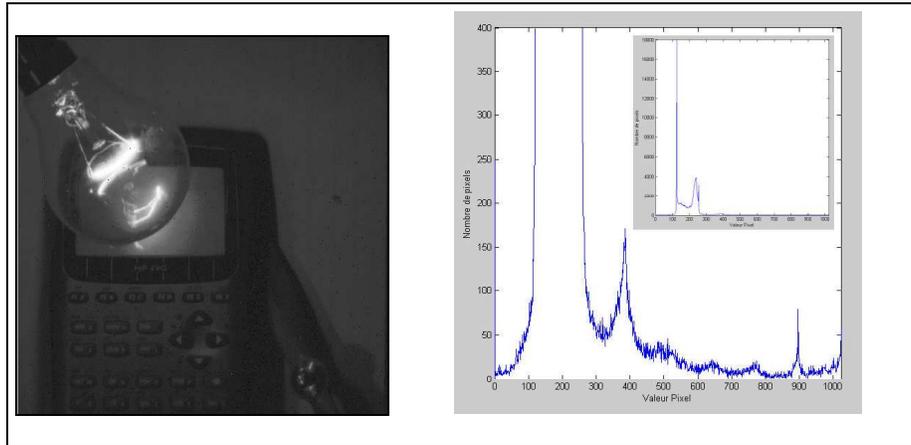
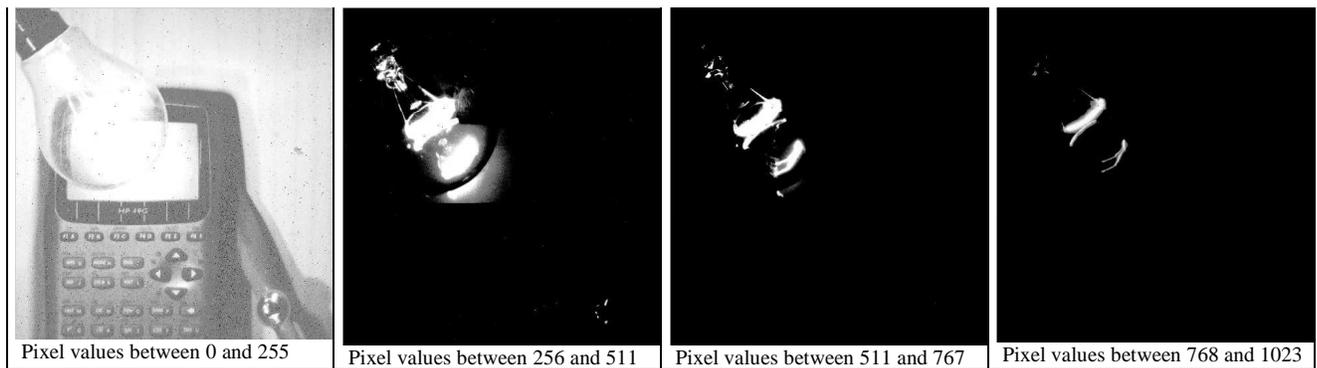


Fig. 9: Image of an HDR scene and the corresponding histogram



The temporal noise have been measured as 7 mV with a significant contribution of KTC noise and comparator noise, the FPN as 6mV and the power consumption as 60mW at video rate.

Efforts are still on-going to improve the behavior of the device. The use of an imaging process would help significantly on this way but the key principles have been demonstrated especially the event based readout principle that allow a unique readout of each pixel along the multiple integrations and the dynamic range extension scheme.

References :

- [1] O. Yadid-Pecht, "Wide dynamic range sensors," *Opt. Eng.*, vol. 38, no.10, pp. 1650–1660, Oct. 1999.
- [2] O. Yadid-Pecht and E. Fossum, "Wide Intrascene Dynamic Range CMOS APS Using Dual Sampling", *IEEE Trans. Electron Devices*, vol. 44, pp. 1721–1724, Oct. 1997.
- [3] M. Mase S. Kawahito, M. Sasaki, Y. Wakamori, "A 19.5b Dynamic Range CMOS Image Sensor with 12b Column-Parallel Cyclic A/D Converters", *ISSCC Dig Tech Papers 2005*, pp. 350-351.
- [4] D. X. D. Yang, A. El Gamal, B. Fowler, H. Tian, "A 640_512 CMOS image sensor with ultra wide dynamic range floating-point pixel level ADC," *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 1999, pp. 308–309.
- [5] L. G. McIlrath, "A low-power low-noise ultrawide-dynamic-range CMOS imager with pixel-parallel A/D conversion," *IEEE J. Solid-State Circuits*, vol. 36, pp. 846–853, May 2001
- [6] A. V. Harton and al, "A High Dynamic Range CMOS Image Sensor with Pixel level ADC and in-situ image enhancement", *Proc SPIE-IST Electronic Imaging 2005*, Vol 5677, pp 67-77
- [7] E. Culurciello, R. Etienne-Cummings, and K. Boahen, "Arbitrated address event representation digital image sensor," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2001, pp. 92–93.
- [8] O. Yadid-Pecht and A. Belenky, "Autoscaling CMOS APS with customized increase of dynamic range", *ISSCC Dig. Tech. Papers*, Feb. 2001, pp. 100–101