

# A 1.75- $\mu\text{m}$ square pixel IT-CCD having a gate oxide insulator composed by a single-layer electrode structure

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## Abstract

We have introduced a gate oxide insulator into a interline transfer CCD (IT-CCD) image sensor by using a single-layer electrode structure. We confirmed that the charge transfer function was not degraded in this structure when subjected to a high electric field, in contrast with conventional gate oxide-nitride-oxide (ONO) structures. We adapted this newly developed structure to a 1.75- $\mu\text{m}$  square pixel IT-CCD image sensor with 8M pixels of 1/2.5-type image format and evaluated its device performance.

## 1. Introduction

IT-CCD image sensor is still the mainstream in compact digital still cameras (DSCs) since CCDs can produce high quality images even for very small pixel sizes. As Fig.1 shows, the pixel size of DSCs has been continuously reduced. The smallest pixel size of IT-CCD image sensors in the 2007 DSC market is 1.75- $\mu\text{m}$  square.

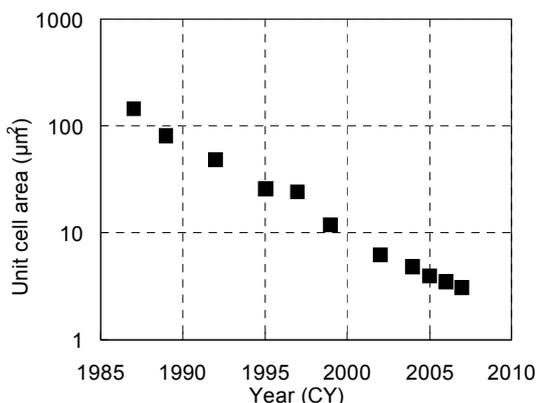


Fig.1 Miniaturization trend of IT-CCD pixel size in SONY.

In spite of a reduction in pixel areas of over 1/40 for the past two decades, the operation voltage of IT-CCD has only been reduced by at most 20%. This is because a high operation voltage is required to maintain a high image quality, in

terms of a high saturation output and a high charge transfer efficiency, etc. Thus, the electric field employed in DSCs is increasing year by year. This is in contrast with the development of general semiconductor devices, which follow a scaling law. We find that, if the electric field in DSCs continues to increase at the current rate, degradation of the charge transfer function will soon become a problem for conventional IT-CCDs constructed with an ONO gate insulator.

We propose the use of gate oxide insulators in IT-CCDs for overcoming this problem.

## 2. Gate ONO insulator on IT-CCD

Over the past two decades, gate ONO structures have been used as insulators for IT-CCD image sensors having multilayer electrodes; one reason for their popularity is that they are convenient from a manufacturing point of view.

As Fig.2 shows, it is difficult to produce a oxide layer having uniform thickness beneath the 1<sup>st</sup> and 2<sup>nd</sup> poly-Si electrodes, because of the necessity of employing a second oxide insulator for a multilayer electrodes having a gate oxide structure. In the case of gate ONO insulator, by adding an oxidizing 1<sup>st</sup> electrode or an oxide

etching step, we can ensure a uniform thickness of the insulator, thereby reducing the ineffective gate voltage swing.

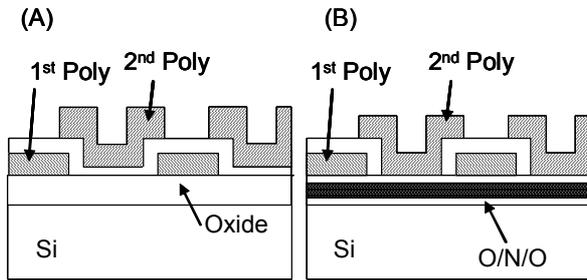


Fig. 2. Cross-sections of (A) gate oxide structure and (B) gate ONO structure and vertical resistor with multi-layer electrode.

However, we found out that such a gate ONO structure potentially can degrade the charge-transfer-efficiency (CTE) due to the high electric field used after charge readout from the photodiode to the vertical register.

Fig.3 shows the shift in the readout voltage as a function of the electric field in a conventional IT-CCD having an ONO gate insulator. This plot indicates that the readout voltage will continue to increase as the electric field is increased. This means that a high electric field will degrade the CTE as the sizes of IT-CCDs are reduced in the future.

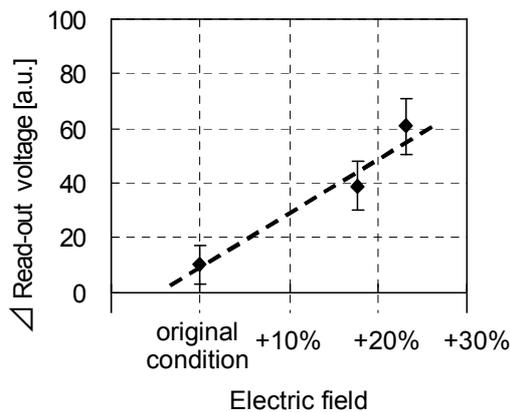


Fig.3 Electric field dependency of  $\Delta$ Read-out voltage. (CTE>0.995)

We developed a hypothesis to explain this phenomenon. Fig.4 shows

a schematic diagram of the cross-section of a photodiode (PD) and vertical register together with the 1D potential profile of IT-CCD during the electron profile read out operation respectively. The gate electrode is positively biased so that accumulated electrons drift toward to the vertical register. At this point, few electrons accelerated by the high electric field can be injected and trapped in the silicon nitride (SiN) layer in the ONO insulator, and this can cause a potential shift as Fig.5 shows.

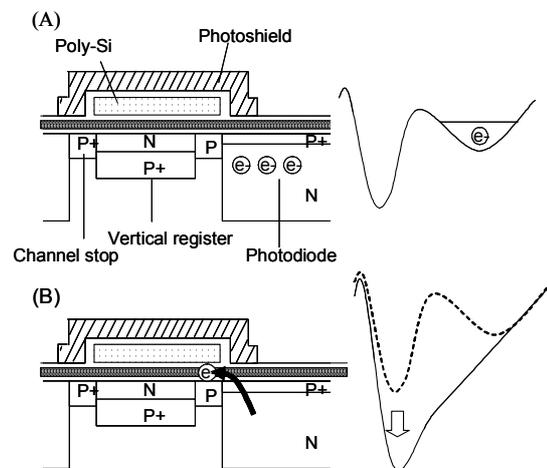


Fig. 4. Schematic of the cross sectional view and 1D potential profile from PD to vertical register during read out operation. (A) At the initial state, PD is fully accumulated by electrons. (B) The gate electrode is positively biased, electrons are flowing toward the vertical layer. Few electrons are injected into SiN layer.

This phenomenon has already discussed for the case of SONOS (polysilicon-oxide-nitride-oxide-silicon) transistors under nonvolatile memory operation [1] [2]. Based on experiments, it is thought that the injection leakage current depends the thickness and electric field across each ONO insulator layer, and a variety of considerable number of different mechanisms occur, including FN tunneling, direct tunneling, modified FN tunneling, and trap-assisted tunneling. The leakage current starts to increase when an electric field of over 5 MV/cm is

applied across a 14.5-nm-thick oxide layer on the silicon [3].

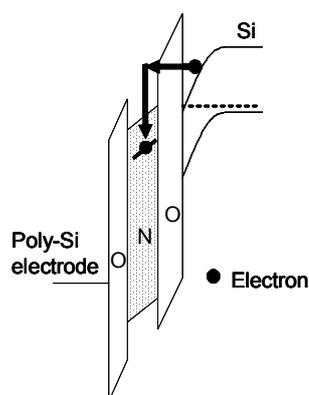


Fig. 5. Energy band diagram depicting electron tunneling and trapping in an ONO insulator.

We found that, even in the case of an IT-CCD having an ONO gate structure that has a thick oxide layer, the possibility of a gate leakage current still exists, and that it can cause significant damage to the charge transfer operation of the IT-CCD when a high electric field is applied.

### 3. Gate oxide structure

We previously developed and evaluated a 2.20- $\mu\text{m}$  square pixel IT-CCD with a single-layer electrode structure. [4] By using such a structure, we could use an oxide layer as the gate insulator for the IT-CCD, without using a SiN layer. The gate insulator is not etched in the etching process steps during gate electrode formation and does not require reoxidation process steps that are required when constructing a second electrode. There is thus only one kind of insulator under the gate electrode in the image area (see Fig.6).

Such a gate oxide structure can reduce degradation of the charge transfer under high-electric-field operation. This is because charge-transfer degradation is caused by the SiN layer in the gate insulator, as mentioned above.

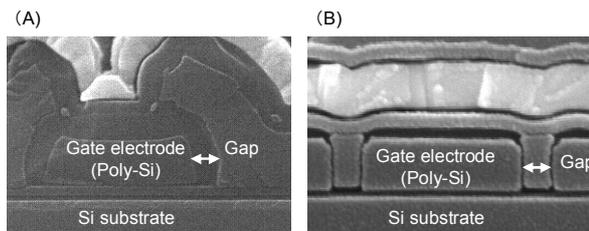


Fig.6 Cross sectional SEM photograph of (A) gate ONO and (B) gate oxide

Fig.7 shows the experimental results obtained. We applied +18% higher biases for charge transfer from the photodiode to the vertical register, and measured the charge transfer efficiency repeatedly. These results show no evidence of charge transfer degradation. We are convinced that gate oxide structures are effective means for overcoming the problem caused by high electric fields, which will become increasingly important as cell sizes are reduced.

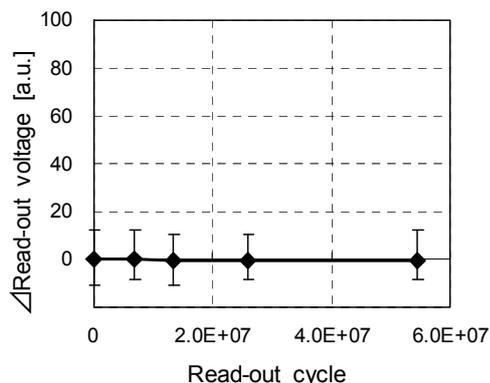


Fig.7 Read-out cycle dependency of  $\Delta$ Read-out voltage. (CTE>0.995)

A further advantage of gate oxide devices is that they have a shorter fabrication process compared with conventional ONO devices. The conventional structure requires more process steps, not just for ONO insulator formation for the CCD, but also for oxide insulators for peripheral transistors, necessary for the deposition and removal steps for the oxide and SiN layers. The gate-oxide-structure CCD proposed in this paper can considerably shorten the

process flow steps due to the multi-oxidation process.

#### 4. Device performance

We have developed a 1.75- $\mu\text{m}$  square pixel IT-CCD image sensor with 8M pixel of 1/2.5-type optical format having a gate oxide structure. The operation conditions used and the device characteristics are shown in Table 1.

The device performance is almost the same as a 2.20- $\mu\text{m}$  square pixel single-gate-electrode IT-CCD. We realized a high performance for a very small cell size IT-CCD that is required to maintain image quality.

Table.1 Specifications and characteristics

| Parameters                                   | Values            |
|--|-------------------|
| Optical format                               | 1/2.5 type        |
| Chip size (mm x mm)                          | 6.616 x 5.486     |
| Total number of pixels                       | 3336×2484 (8.29M) |
| Number of active pixels                      | 3298×2472 (8.15M) |
| Pixel size ( $\mu\text{m}$ x $\mu\text{m}$ ) | 1.75 x 1.75       |
| Horizontal clock rate (MH)                   | 36                |
| VDD / Read-out bias (V)                      | 13/13             |
| vertical transfer / horizontal transfer (V)  | -7.5 / 3.3        |
| Saturation output (mV)                       | 420               |
| Sensitivity (mV/Lux)                         | 165               |

#### 5. Conclusions

A single-layer electrode IT-CCD image sensor having a gate oxide insulator has been developed and applied to a 1/2.5-type 8M pixel high resolution IT-CCD image sensor. We confirmed that there was no degradation of charge transfer for this device, in contrast with ONO gate IT-CCDs. The performance of this newly developed device is very suitable for application to small-pixel image sensors and further reduction in pixel size. This advantage is especially relevant for small pixel sizes, in this study enabling a 1.75- $\mu\text{m}$  square pixel IT-CCD.

#### 6. Acknowledgement

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#### 7. Reference

- [1] J. H. Yi, H. Shin, Y. J. Park, and H. S. Min “Polarity dependent device degradation in SONOS transistors due to gate conduction under nonvolatile memory operations” IEEE Trans. Device and Materials Reliability, vol. 6, pp. 334 – 342, 2006
- [2] S. Mori, et. al. “ONO inter-poly dielectric scaling for nonvolatile memory applications” IEEE Trans. Electron Devices, vol. 38, pp. 386 – 391, 1991
- [3] M. Aminzadeh, S. Nozaki, and R. V. Gridihar, “Conduction and charge trapping in polysilicon-silicon nitride oxide-silicon structures under positive gate bias,” IEEE Trans. Electron Devices, vol. 35, no. 4, pp. 459-467, 1988
- [4] N. Karasawa, et. al. “A 2.20- $\mu\text{m}$  square pixel IT-CCD constructed from single-layer electrode” IEEE Workshop on CCD and Advanced Image Sensor, pp. 210-213, 2005