A 3Mega-Pixel back-illuminated image sensor in 1T5 architecture with 1.45µm pixel pitch

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Abstract:
A 3Mega-Pixel back illuminated image sensor in 1T5 architecture and 1.45µm pixel pitch has been successfully developed and characterized. A high quantum efficiency over 60% in the visible light spectrum and a low dark current of 1e$^-$/s at 25°C have been achieved due to dedicated frontside and backside process steps such as antireflective layer adaptation, p$^+$ pinning layer and thermal treatment.

Introduction:
CMOS image sensors are gaining a high influence since several years. The main challenge consists in shrinking the pixels without decreasing the pixel performances, as the optical stack and the metal wiring over the surface reduced diode cause optical efficiency issues [1, 2]. The realization of a back-illuminated image sensor offers a fundamental solution, as the backend stack is located under the photodiode [1-3]. We demonstrate a 3 Mega-Pixel back-illuminated image sensor with a 1.45µm pixel pitch in 1T5 architecture, which has a mean dark current of 1e$^-$/s at 25°C and a quantum efficiency (QE) of over 60% in the visible light spectrum.

Pixel Design:
The backside illuminated 3MP image sensor with a 1.45µm pixel pitch has been realized in a 0.13µm front-end CMOS based process. The backend metallisation was processed in 90nm copper based design rules [4]. The principal pixel architecture is a pinned fully depleted noiseless photodiode with transfer gate and reset noise cancellation thanks to correlated double sampling (CDS). Several transistors are shared between neighbouring pixels, resulting in 1T5 pixel architecture [4]. A pixel schematic is shown in figure 1: each pixel has a diode and a transfer gate transistor (TG). In order to increase the fill factor, four pixels are regrouped to one sensing node, which is connected to a reset (RST) transistor and to a source follower (SF) transistor.

Process& Experiments:
The process is realized on silicon on insulator (SOI) starting material. Several SOI thicknesses have been evaluated in order to find an optimum between quantum efficiency and crosstalk.

Dedicated p$^+$ implants are implanted in the pixel area. A vertical p$^+$ implant isolates the pixels from each other, resulting in a lower crosstalk and higher quantum efficiency. Figure 2 shows a relative increase of 20% quantum efficiency with the introduction of the specific p$^+$ implant. In a standard CMOS imager the diode surface potential is pinned to 0V and the photogenerated holes are evacuated by the substrate. On the SOI substrate the diode surface pinning and the hole-evacuation is provided by an additional contact on a p$^+$ implant. The backend consists in 3 metal layers. As the chips are illuminated from the backside, metal lines are allowed to cross directly above the diode area [3]. Furthermore the dielectric backend stack does not have to be optically optimized in terms of total thickness and material composition. After the final metal layer, a passivation layer and subsequent wafer bonding layer (WBL) are deposited. The WBL is planarized and a support wafer is bonded to the processed wafer. Afterwards the processed wafer is back-grinded. The backside surface is covered by an antireflective coating in order to avoid light losses by reflections. Figure 3 shows the simulated transparency with and without antireflective layer. The pads are reopened through the active silicon layer and finally deposited and patterned aluminium in the pads provides a standard surface for test and package purposes. In the next development steps color filters will be realized on the sensor, which is monochrome without micro-lens for the time being. The process flow is summarized in figure 4.

Pixel performances:
The conversion gain of the image sensor is 66µV/e$^-$. The quantum efficiency (QE) has been evaluated as a function of the SOI thickness. Figure 5 shows that a QE gain for wavelength >460nm can be observed for a thick SOI layer, as too thin silicon layers cannot absorb the entire light quantity of longer wavelength according to the absorption law. The Modulation Transfer Function (MTF) for different wavelengths is presented in figure 6. A decrease of the MTF, which is equivalent to an increased crosstalk, can be observed for shorter wavelengths. As the blue light is absorbed near the surface, the photogenerated electrons have to cover a longer distance in order to reach the diode and thus have a higher possibility to

diffuse into the neighbouring pixels, which increases the crosstalk. A decreased crosstalk, which corresponds to a higher MTF, can be reached by a lower substrate thickness, as shown in figure 7. In comparison to figure 5 we can conclude, that a compromise for the substrate thickness has to be made up in terms of pixel crosstalk on the one hand and QE on the other hand. Thicker substrates increase the QE, whereas the crosstalk increases, too.

The full well diode saturation charge is reached at $4000e^-$. An improvement of the saturation could be obtained by diode doping profile optimization. The dark current is $1e^-$/s at 25°C. Figure 8 shows the dark current as a function of temperature. The low dark current has been achieved thanks to dedicated frontside and backside process steps such as p^+ pinning layer and thermal treatment. Due to a very good charge transfer, the lag is below the measurement threshold. The temporal noise measured in darkness is $5e^-$, the main contributor being the source follower transistor. The principal image sensor parameters are summarized in table 1.

Figure 9 shows a picture, taken by the 3MP back illuminated image sensor with 1.45µm pixel pitch in 1T5 architecture.

Conclusion:

We have demonstrated the feasibility of manufacturing CMOS image sensors with a very small pixel pitch (1.45µm x 1.45µm) in a back illuminated process. A high QE of 60% in the visible light spectrum has been reached. Other image sensor parameters like the conversion gain, the dark current, the lag and the temporal noise have not been deteriorated by the backside process and are comparable to state of the art standard frontside image sensors.

Ongoing work is related to the crosstalk reduction as well as color filter and micro-lens processing.

Acknowledgements:

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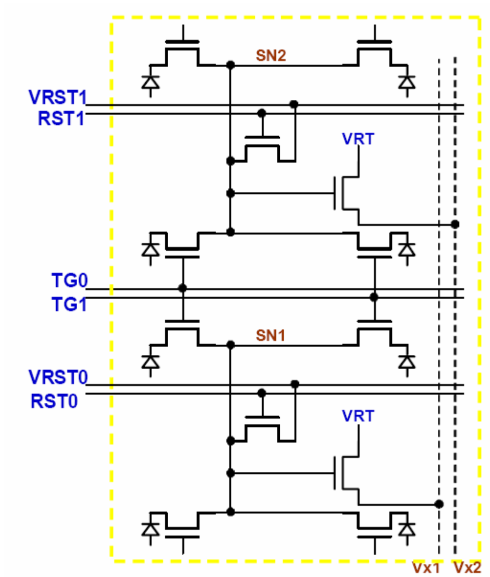

Fig. 1: 1T5 pixel schematic

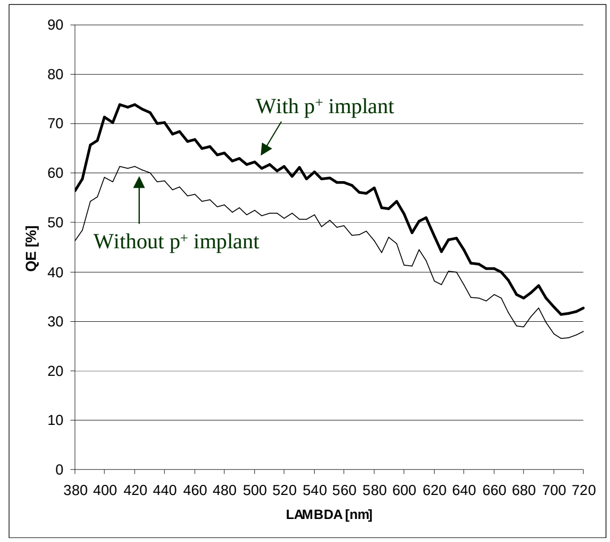

Fig. 2: Influence of p^+ implant on QE

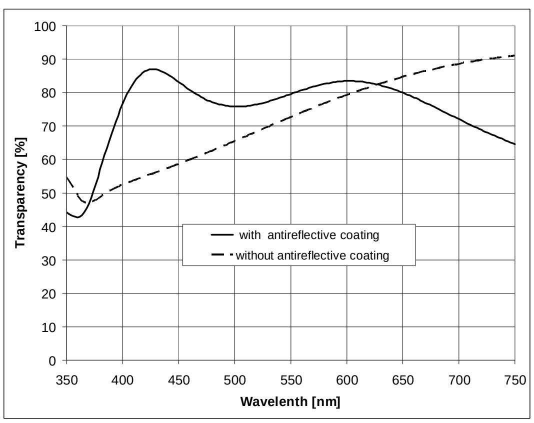

Fig. 3: Transparency with and without antireflective coating

- SOI wafer
- CMOS Imager Process
- Wafer Bonding Layer (WBL) Deposition and Preparation
- Wafer bonding and backside grinding
- Anti-reflective-coating (ARC)
- Pad opening
- (further development: Color Filters and Micro-Lens)

Fig. 4: Process flow

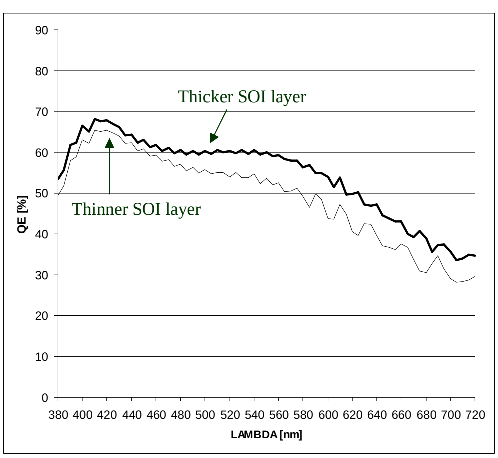

Fig. 5: Influence of SOI thickness on QE

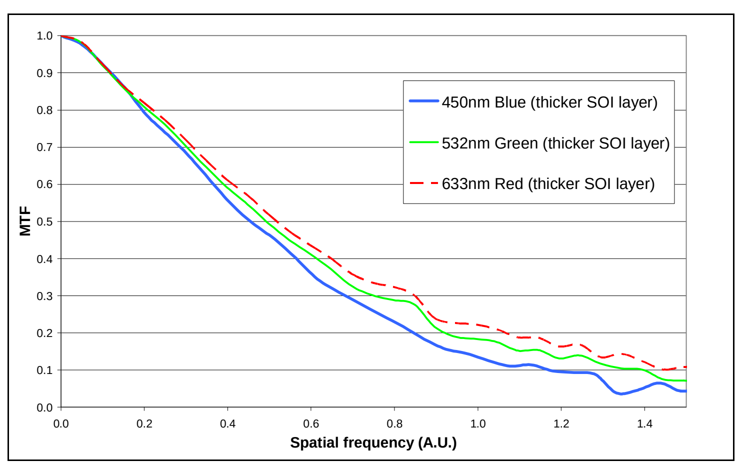

Fig. 6: MTF for thicker substrates at different wavelength

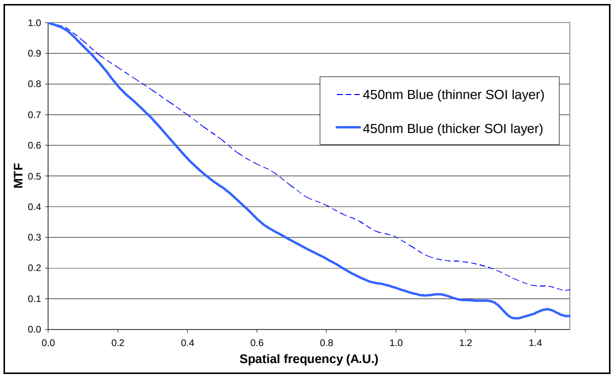

Fig. 7: Comparison of MTF at 450nm for thinner and thicker substrates

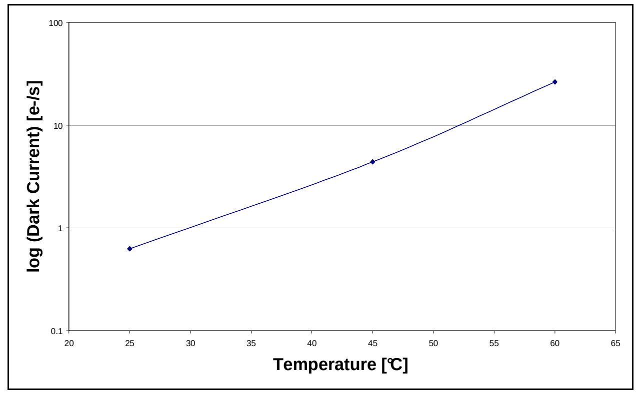

Fig. 8: Temperature dependence of dark current

	1.45µm back illuminated pixel	Comment
Saturation charge [e-]	4000	Full Well
Conversion Gain [µV/ e-]	66	
Lag [e-]	0	Charge transfer free of lag
Sensitivity[e-/ Lux s]	6800	3200K + IR cut-off at 650nm
Dark Current at 25°C [e-/s]	1	Mean Value
Temporal Noise [e-]	5	Main contributor: SF
Quantum Efficiency @ 550nm [%]	60	

Table 1: Summary of 1.45µm back illuminated pixel performances

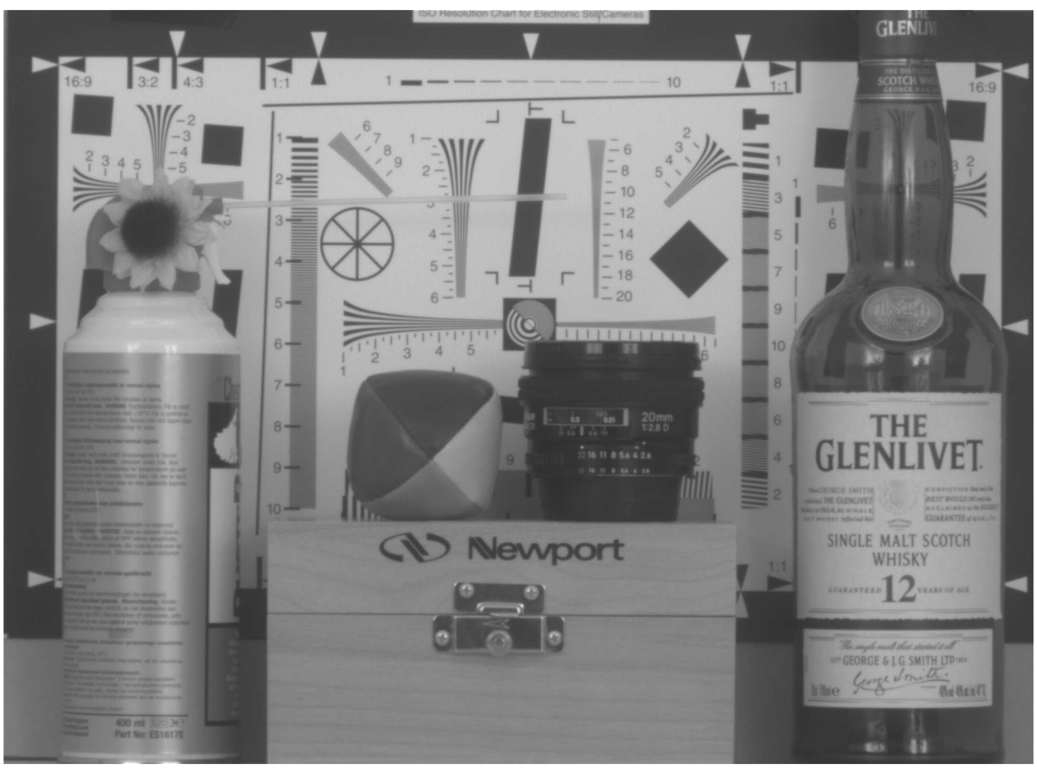

Fig. 9: Monochrome image from 3MP back illuminated array with 1.45µm pixel pitch