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A Wide-VGA CMOS Image Sensor with Global Shutter and Extended Dynamic Range

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Abstract

This paper describes a wide-VGA format (752 x 480) CMOS image sensor that targets various automotive "scene processing" applications, such as occupant classification systems, lane departure warning, and blind-spot detection. The sensor runs at 60 fps.
The chip size is 6.3mm (H) x 5.7mm (V). The sensor features global shutter, extended dynamic range along with automatic gain, automatic exposure control, and tiled digital gain. It has column-parallel ramp ADC architecture. The sensor operation, architecture, and characterization results are discussed in the article.

1. Introduction

The sensor was designed to operate in adverse environments (wide temperature range and extreme light conditions), which is an essential requirement for the automotive industry. It is sensitive to the visible and near IR spectrum of light. The sensor has a global shutter pixel architecture. The pixel is a five-transistor (5T) type buried photodiode laid out in a 6μm pitch for better sensitivity. Extended dynamic range is achieved through a programmable piecewise non-linear pixel response. Global shutter and in-pixel high dynamic range techniques were previously only implemented for regular photodiode pixels [1, 2, 3].

2. Pixel Operation

Figure 1 shows a schematic of the five-transistor type active pixel that is used in the sensor. The pixel consists of a buried photodiode (PD), pixel memory (storage node M) and five transistors for pixel reset and readout. The AB gate controls reset of the photodiode. This reset is global and allows a new integration period to start independently during the pixel memories readout. Complete charge transfer is required here. The TX gate controls global shutter operation and enables high dynamic range mode (HiDy). Incomplete charge transfer due to a barrier under the TX gate may result in lag and high FPN. The RST gate provides pixel memory reset and controls pixel saturation level in the HiDy mode. Step voltage is applied to the RST gate during HiDy operation. Double-knee programmable piecewise pixel response allows extended dynamic range up to 16 f-stops. Automatic knee control preserves the chosen pixel response when shutter width varies.

The pixel operation sequence is shown in Figure 2. There are two major phases of pixel operation. The first is the readout phase; during this phase the PD gets reset and then accumulates signal charge afterwards and at the same time the pixel memories are read out row by row. The second phase is the HiDy operation and charge transfer; during this phase the shutter is open and signal charge spills into the pixel memory. In HiDy mode a barrier is built up under the RST gate. There are three steps of voltage applied to the RST gate that correspond to two knees on the pixel response curve. The barrier height variation can result in FPN that could make the dynamic range extension ineffective. A soft reset of the pixel memory cancels thresholds of individual transistors, and a flushed reset helps to get rid of soft-reset-related lag. Pixel memory capacitance mismatch is another potential source of FPN at each knee point. It was minimized by proper choice of pixel operation and pixel parameters.
Figure 3 shows the concept of frame timing. Frame time includes pixel memories readout and vertical blanking time. We cannot perform HiDy operation during pixel memories readout, so HiDy operation takes place during the vertical blanking time, which is typically 37 rows. The intra-scene dynamic range extension is proportional to the time ratios of T1/T2 or T1/T3. T1 normally is much more than (T2 + T3). Global shutter operation prohibits the use of true CDS. Therefore, pixel-memory-reset kTC noise contributes to temporal noise. There is an advantage to using the buried photodiode that allows us to get rid of the kTC noise related to the reset of the PD and the charge transfer into the pixel memory. Another advantage of using the buried photodiode is the reset of the PD, which does not require flush for lag suppression. This works if we achieve a complete charge transfer.

3. Sensor Architecture

The sensor block diagram is presented on Figure 4. The sensor has a column-parallel ramp ADC architecture. Every column includes a switched capacitor unity gain inverting amplifier, switched capacitor programmable gain amplifier, two-stage comparator, and DRAM. The analog signal chain is similar to the one described in [4]. It is simple and allows us to achieve low temporal noise and low column FPN. Another advantage of this architecture is the low power consumption and speed. The two-port memory is arranged as parallel-in/serial-out. The front-

end memory stores the ADC output data from the current row during readout and simultaneously outputs the data of the previous row. While the pixel signal is sampled, the amplifiers and comparator are reset, and then the pixel reset is sampled when the feedback switches are turned off. The voltage difference (Vreset-Vsignal) gets amplified by the PGA and is stored on the SH capacitor. The PGA output signal is positive. In conversion time this signal gets compensated by a negative ramp. A good feature of this readout circuit is the capability of noise cancellation, which was represented earlier in [4].

The ADC resolution is 12-bit. A companding scheme of 12-bit into 10-bit is implemented in the ramp generator, which allows enhancement of the contrast by using the full ADC resolution at low light while sacrificing high light resolution. The ADC resolution is not so critical at high light because of the high level of photon shot noise. The 12-to-10-bit companding scheme is presented in Figure 5.

Histogram-based auto exposure (AEC) and auto gain (AGC) controls are integrated on the chip. The image can be divided into 25 tiles. Each tile has an individual digital gain of 0.25–3.75x. The image grid allows the user to identify tiles of interest upon which the AEC/AGC unit performs its computations. The user can, therefore, force the AEC/AGC unit into just using pixels from a region of interest. Since the region of interest is fully flexible (grid coordinates can be arbitrarily changed) and each tile can be given an arbitrary weight (0–15), an object that is backlit or shaded can be selected for good viewing at the expense of the remainder of the image.

The sensor has a parallel 10-bit output and an alternative serial LVDS output. The LVDS serial output can transmit data from a single standalone sensor or stream-merged data from two sensors (self and its stereoscopic slave pair). The stereoscopic topology is shown in Figure 6. In this configuration an on-chip PLL generates a shift-clk (x18) in phase with the 27 MHz system clock. An external deserializer can be used to retrieve the output data from each sensor. The sensor output syncs are embedded in the pixel data stream.

An integrated digital thermometer records the sensor temperature every frame and can be read out through the control interface.

4. Characterization Results

The sensor was fabricated in 0.18μm 2P3M CMOS sensor process. The sensor spectral range covers 400–900nm with QE > 25%, as shown on Figure 7. The response is enhanced in the near IR range. A responsivity of 4.8 V/Lux*s for dynamic range of 60dB is achieved. Dark temporal noise is about 22e-, which is primarily caused by kTC noise related to reset of pixel memory. Flushed reset increases kTC noise. SNR at mid and high signal levels is limited by pixel FPN. The primary source of pixel FPN is the variation of charge transfer from buried photodiodes. The SNR reaches 37dB in linear mode at 25C. High dynamic range mode permits dynamic range extension up to 100dB. The key limitation here is pixel FPN, which determines SNR at high lights. Performance also degrades with temperature growth, but the HiDy response is insensitive to temperature. Pixel FPN at 85C is determined by dark current variation. For illustration, in Figure 8 a high dynamic range scene was captured in linear and HiDy modes. Each half of the chart shown in the image gets different illumination.

The sensor shutter efficiency is 99.5 percent. It was found that leakage to pixel memory does not depend on charge accumulated in the photodiode but does depend upon the light intensity, which means that the photoelectrons generated in the depth of the substrate are involved in the leak.

Charging and discharging lag is less than 1 percent. Full charge transfer and flushed pixel memory reset contribute to this low level.

The sources contributing to pixel dark current are photodiode dark current, pixel memory leak, and charge generation under TX gate. The pixel memory leak contributes most of the dark current, but PD component becomes dominant at 85C. The total pixel dark current is about 14 mV/s at 25C.

5. Summary

A wide-VGA CMOS image sensor with global shutter and extended dynamic range is presented in this paper. The sensor pixel array is featuring buried photodiode. The sensor targets the automotive application camera market together with multiple machine vision applications.

Acknowledgements

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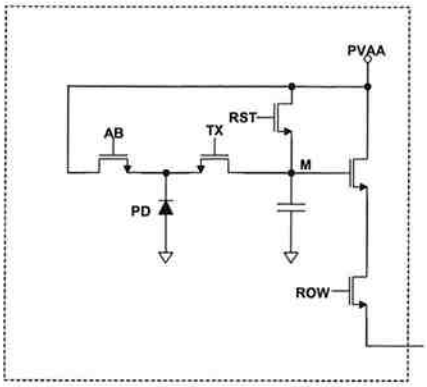

Figure 1. Schematic of pixel.

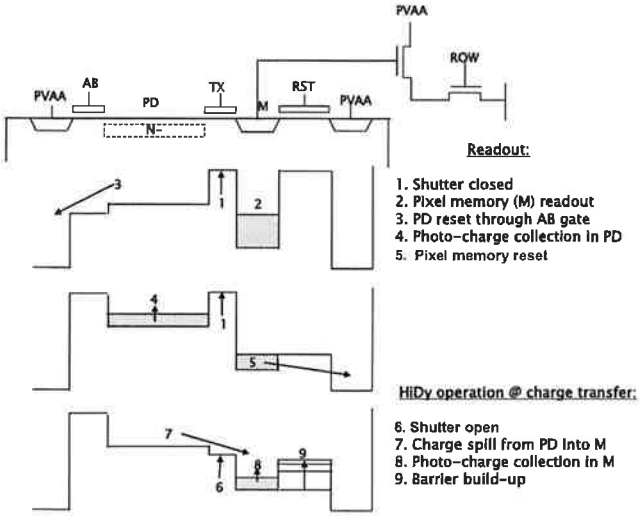

Figure 2. Sequence of pixel operation.

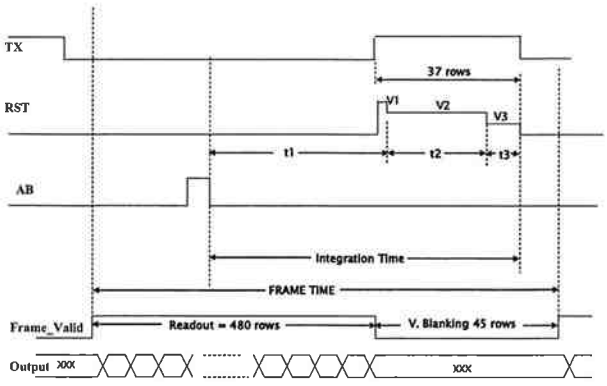

Figure 3. Concept of frame timing.

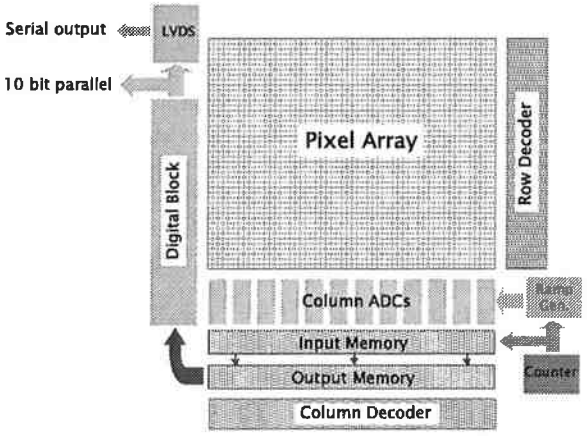

Figure 4. Sensor block diagram.

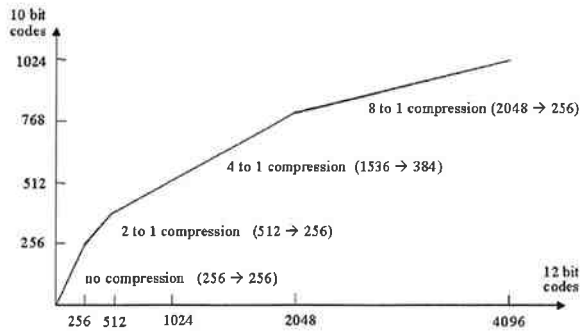

Figure 5.12-to-10-bit companding scheme.

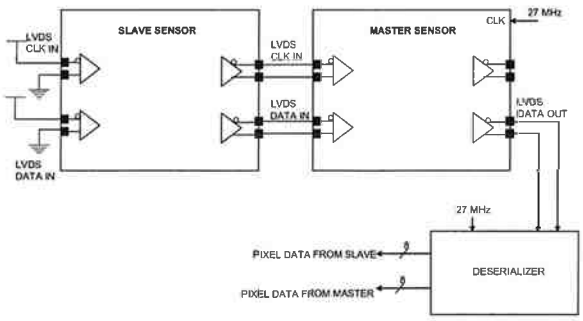

Figure 6. Configuration of sensor for stereoscopic serial output.

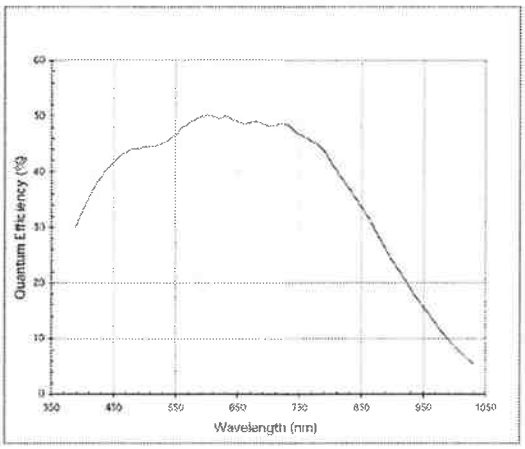

Figure 7. QE of the MONO sensor.

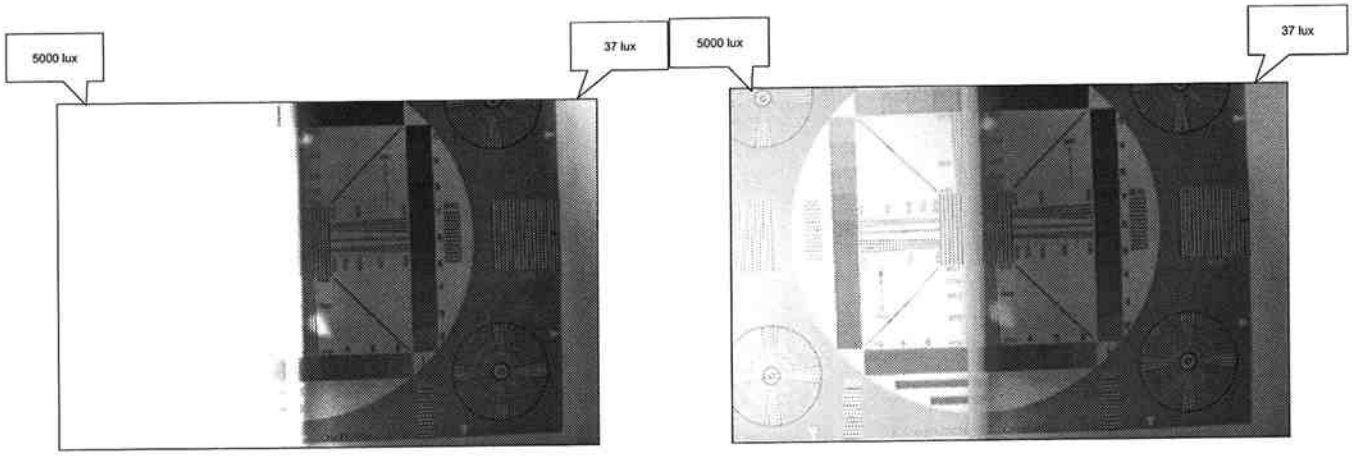

Figure 8. Image of TV chart in linear (left) and HiDy (right) modes.

Table 1. Sensor parameters.

Technology	0.18µm 2P3M
Chip Size	6.3mm (H) x 5.7mm (V)
Array Size	752(H) x 480(V)
Optical Format	1/3 inch
Frame Rate	60 fps at full resolution
Shutter Type	Global Shutter
Supply Voltage	3.3V
Power Consumption	190mV @ 60 fps
Operating Temperature	-40C to +85C
Color	Mono or RGB Bayer Pattern
Pixel	6µm @ 5T buried photodiode
Spectral Range	400–900nm @ QE >25%
QE	48% @ 550nm, Mono + u-lenses
Responsivity	4.8 V/Lux*s
Pixel Conversion Gain	57uV/e-
Temporal Noise	22e-
Pixel Saturation	30000e-
DSNU	0.07% sat. (r.m.s.)
PRNU	0.7% at ½ saturation (r.m.s.)
Charging/Discharging Lag	<1%
Dark Current	14mV/s at 25C
Dynamic Range	Linear: 60dB; Extended: 100dB
Shutter Efficiency	99.5%
ADC DNL, INL	DNL: <0.6 LSB; INL: <1LSB