

## Optical-electrical characteristics of small, sub-4 $\mu\text{m}$ and sub-3 $\mu\text{m}$ pixels for modern CMOS Image Sensors

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### Abstract

This paper describes a 4TC pixel for CMOS image sensors. This pixel features improved linearity and pixel capacity, high quantum efficiency and low crosstalk, providing superior image quality and sensitivity in mobile applications. We present results of optical and electrical characterization of 3 pixels and pixel array generations, compare critical parameters and characteristics for pixels with different sizes (from 5.6 $\mu\text{m}$  to 1.7 $\mu\text{m}$  pixel pitch), and present crosstalk data for pixels optimized for different angles of incident light. Experimental data is compared with results of modeling and simulation.

### Introduction

Industry trends in modern CMOS image sensor design have included the reduction of the optical format and an increase in total sensor resolution. At the same time, the modern mobile applications of image sensors demand image quality approaching that of a DSC. This requires shrinking pixel size to the range of 2 $\mu\text{m}$  – 3 $\mu\text{m}$  and smaller while maintaining high pixel capacity, high responsivity, high quantum efficiency, and low crosstalk. As pixels shrink, to accommodate the conflicting demands of higher resolution and smaller optical format, trade-offs must be made in order to maintain performance.

### Pixel architecture and process description

Figure 1 shows basic 4TC in-pixel capacitor architecture [1, 2]. Improved linearity and pixel capacity is achieved by adding a low-depletion poly/nitride/poly capacitor on the small-area floating diffusion (FD) node. The conversion gain of the FD can be tuned by changing the value of the in-pixel capacitor to achieve a trade-off between low-light sensitivity and full-well capacity for the best overall performance. The 4TC architecture with true correlated double sampling improves read noise performance over past 3T architectures.

Reduced pixel size results in significant reduction of pixel capacity and corresponding signal to noise ratio (SNR). To preserve pixel capacity for small pixels we used a common element pixel architecture (CEPA) with 2.5 equivalent transistors for pixels smaller than 4.2 $\mu\text{m}$ , and 1.75 and 1.5 equivalent transistor for pixels smaller than 2.6 $\mu\text{m}$ . Micron's CMOS Imager process utilizes a 2-Poly, 3-Metal process with .18 $\mu\text{m}$  min features for 5.6 $\mu\text{m}$  to 4.2 $\mu\text{m}$  pixels, .15 $\mu\text{m}$  min features for 3.6 $\mu\text{m}$  to 2.8 $\mu\text{m}$  pixels, and .13 $\mu\text{m}$  min features for 2.6 $\mu\text{m}$  to 1.7 $\mu\text{m}$  pixels. Figure 2 shows pixel capacity for 3 pixel generations and corresponding process features.

Micron's transistor process has been optimized for speed and reliability at 3.3V, 2.8V, and 1.8V modes of operation. At higher operating voltages, the transistor design rules, implants, and thermal annealing processes have been tailored for improved channel hot carrier reliability. Implant engineering of the transfer gate transistor was done to minimize lag, reduce dark current/hot-pixel defects, and improve pixel FPN. Shallow Trench Isolation and PWell processes were modified to further reduce dark current and electrical cross-talk, while optical crosstalk benefited from Micron's reduced stack height (photo-diode to CFA distance). Layout and process optimization of the photo-diode (PD) has resulted in improved fill factors and higher full-well capacity while

maintaining low dark current and low electrical cross-talk. Thousands of pixels layouts and process combinations were studied to optimize each pixel generation.

### Pixel development and test vehicle design

Micron uses a fully functional optical array (FFOA) to test new pixel geometries (both pixel design and process development). Each FFOA contains an array of pixels comprised of certain design features that are of potential interest for future products. These design features include pixel pitch, pixel layout, number of metal layers, number of row and column lines, etc. To allow for maximum flexibility in pixel control, the periphery circuits contain no digital block or DACs. Our external hardware provides all of the timing, voltages, and currents, allowing us to completely control the pixel array and to determine the required stimulus for the pixels under consideration.

### Color filter and microlens process, pixel arrays with microlens shift for non-telecentric applications.

The color filters are built with standard negative color resists using a process optimized for improved cross talk and across die uniformity. Special precautions are taken to avoid visible streaks or blemishes. To maximize angular light acceptance of the pixels, the process does not use planarizing layers.

A square cushion shaped micro lens on each pixel increases quantum efficiency and reduces cross talk. The microlenses are formed lithographically using photo-imageable transparent photo resist, followed by a reflow process. To maximize the optical performance of very small pixels, a gap-less microlens process has been implemented, providing superior light focusing and near 100-percent area collection efficiency. Figure 3 presents an SEM scan of microlenses with about 98-percent area coverage for a 1.7 $\mu\text{m}$  pixel array.

The color filter / microlens stack has demonstrated good stability against thermal and UV light stress. Once cured, the microlenses have been shown to be stable against shape changes under the conditions required for the reflow of lead-free solder pastes (e.g. 260°C).

Image sensors for mobile applications require special optimization of the color filters and micro lens array. Using the technique described in [3] the position of the color filter and micro lens for each individual pixel in the array has been optimized for the corresponding chief ray angle (CRA) of incident light. Optimization of color filters and micro lens allowed us to achieve a maximum CRA of 25 degrees for 3.6 $\mu\text{m}$  pixels and ~20 degrees for 2.2 $\mu\text{m}$  pixels. Signal degradation and color distortion do not exceed 10% and 3% for 3.6 $\mu\text{m}$  pixel arrays, and correspondingly 15% and 4% for

2.2 $\mu\text{m}$  pixel arrays. Further optimization of the microlens design will allow further reduction of color distortion for small pixels.

### Results of optical and electrical characterization.

Optical and electrical characterization of pixels was performed using both sensor design and test pixel array vehicles design.

Pixel capacity is one of several important characteristics of image sensors that affect the image quality and signal-to-noise ratio (SNR) under high light conditions. Scaling of photodiode size and operating voltages present many challenges for maintaining pixel capacity. In our pixel development we have tried to maximize pixel capacity for small pixels using CEPA design, in-pixel capacitance, and optimization of PD implants to equalize the capacity of the PD and FD. Figure 4 presents predicted and experimental results of pixel capacity for different pixel sizes and 2.8V operating voltage. Pixel capacity is more than 25ke for 3.6 $\mu\text{m}$  and larger pixels, 10ke - 17ke for pixels in the range from 2.0 $\mu\text{m}$  to 2.8 $\mu\text{m}$  and about 9ke for 1.7 $\mu\text{m}$  pixels.

Dark current is another important characteristic of CMOS image sensors affecting low light performance. Achieving a low dark current is extremely important for small pixels because of limited pixel capacity. Figure 5 presents dark current at 55°C for pixels of different sizes. Dark current is equal to 300 e/s at 55°C for the large 5.6- $\mu\text{m}$  pixel and goes down to 30 e/s for the 2.8 $\mu\text{m}$  pixel and 20 e/s for the 2.2 $\mu\text{m}$  pixel. Dark current normalized to pixel area (solid line on the Fig. 5) shows dark current improvement during the development of 3 generations of pixels. While this dark current remains above the best CCD performance, the low-light performance for reasonable integration times (< 1 second) is limited by photon shot noise or several electrons of read noise at extremely low light conditions. Typical distribution of dark current at 55°C for a 2 Mpix image sensor with 2.8 $\mu\text{m}$  pixel size is shown on the Figure 6a. The solid line represents the histogram of dark current distribution within the array; the dotted line represents cumulative histogram. The quantity of hot pixels exceeding 10x of average value of dark current is less than 0.7 %. Figure 6b presents dark current as a function of temperature for the same pixel. Activation energy depends on the concentration of PD implants and was measured in the range from 0.93 eV to 1.03eV for devices with different PD processes, indicating that the primary contributor to dark current is diffusion current from the bulk substrate.

Typically, lag performance has been cited as a major concern for CMOS imager sensors. The problem with lag becomes increasingly difficult as pixel size shrinks and concentration of PD implants increases to preserve the full well capacity of the smaller PD area [2]. The pixel design and process were simultaneously optimized to achieve low lag for each pixel generation. Figure 7 shows simulation of semiconductor potential during charge transfer from the PD via the Transfer Gate (TX) to the FD node, made using Silvaco™ Athena and Atlas software (a) and lag for 4.2 $\mu\text{m}$ , 3.6 $\mu\text{m}$ , and 2.2 $\mu\text{m}$  pixels (b). Lag is less than 0.03% for 40% of saturation and less than 1% for 1% of saturation.

Crosstalk in image sensors degrades low light performance and creates additional noise after color processing at normal light conditions. The low stack height of the dielectric layers

as well as an optimized process provide high quantum efficiency and low crosstalk for these pixels. Figure 8 presents the spectral characteristics and crosstalk data for a 2.8 $\mu\text{m}$  pixel array measured with f/2.8 incident light in accordance with the technique described in [3]. The center of the array is optimized for normal incident light, and corresponding spectral characteristics are presented in Figure 8a. Pixels on the horizontal edge of the array are optimized for the chief ray angle of incident light CRA ~ 20 degrees. Spectral characteristics and crosstalk of those pixels under the incident light with CRA=20 degrees are shown in Figure 8b. Sensor exhibits high (close to 40%) QEmax both for green and blue pixels as well as small crosstalk. Reduction of QE for peripheral pixels illuminated with angled light is less than 15 percent. Increase of crosstalk is about 10 percent.

Table 1 summarizes important optical and electrical characteristics of our pixels for mobile applications. The responsivity changes from 2.8V/lux-s for a 5.6 $\mu\text{m}$  pixel to 0.32V/lux-s for a 1.7 $\mu\text{m}$  pixel. The pixel capacity is about 30ke for the biggest 5.6- $\mu\text{m}$  pixel, providing the maximum SNR of 44.7 dB. Pixel capacity of the smallest 2.2 $\mu\text{m}$  and 1.7 $\mu\text{m}$  pixel is 11.8ke and 9.0ke providing SNRmax close to 41dB and 40dB respectively. The noise floor determined by image sensor design varies from 8 equivalent electrons for image sensor based on 5.6 $\mu\text{m}$  pixels to 3 equivalent electrons for the smallest pixels. The corresponding pixel dynamic range is about 70dB.

Shrinking the pixel size results in a reduction of sensitivity in low light conditions. To illustrate this trend, we estimated the noise equivalent scene illuminance (NESI) for a given optical system and integration time. Figure 9 presents NESI for different pixel sizes. The following noise components were used in this estimation: pixel and analog chain readout noise, photon shot noise, and noise of accumulated dark charge at 35C. In spite of significant progress in pixel development and reduction in readout noise, sensor sensitivity is reduced when pixel shrinks. NESI for the 1.7 $\mu\text{m}$  pixel is 6x of NESI for the 5.6 $\mu\text{m}$  pixel. On the other hand, the 6x sensitivity drop is not that large compared to the 10x that can be expected from a simple area scaling factor. The difference being the substantial process and readout improvement during the development of 3 generations of pixels. A reasonable quality color image produced with Micron's 1.7 $\mu\text{m}$  pixel array can be seen in Figure 10.

### Conclusion

Micron pixels and pixel arrays designed for mobile applications cover a wide range of device optical formats and total resolution. Using CEPA designs, an optimized process with .13 minimum features, and an advanced CFA/microlens process has allowed pixels as small as 1.7 microns to maintain high pixel capacity, high QE, low crosstalk, and achieved high quality images.

### Acknowledgements

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### References

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- [2] H. Rhodes et al. IEEE Workshop on Microelectronics and Electron Devices, pp. 7-18, 04 2004
- [3] G. Agronov et al, Trans. ED, ED-50, 2003, pp.4-11.

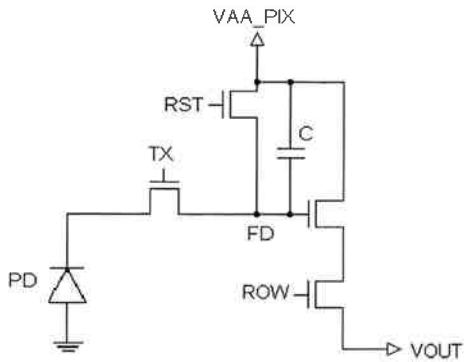


Figure 1. Basic 4TC pixel architecture

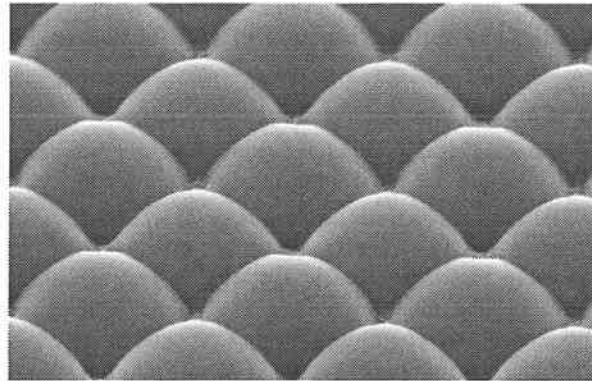


Figure 3. Micro lenses for 1.7-um pixel array

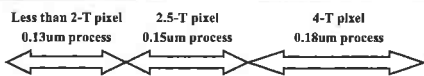
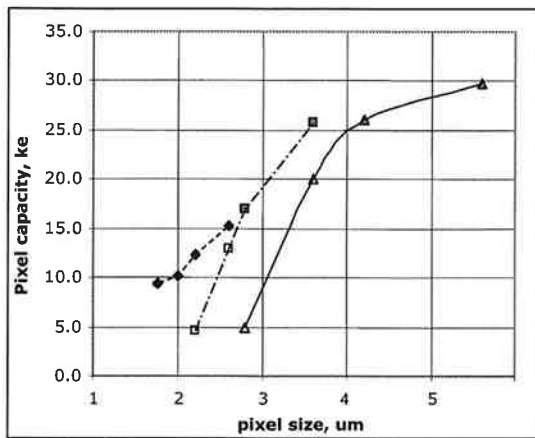


Figure 2. Pixel generation and process features

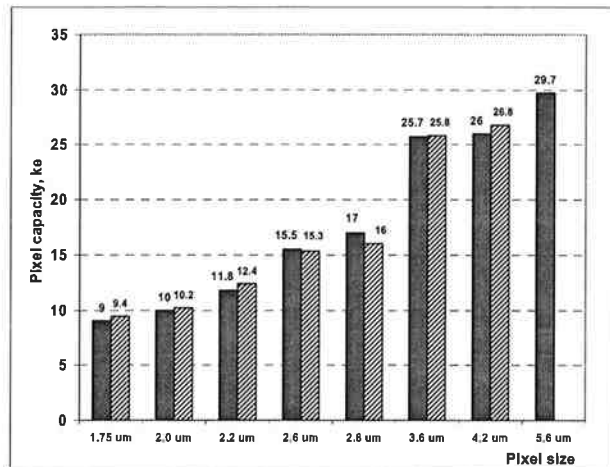


Figure 4. Pixel capacity (linear signal range) for pixels with different size.

Experimental data  
Simulation results

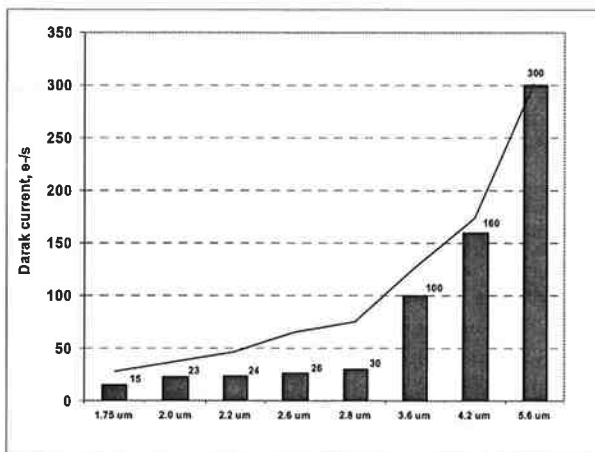


Figure 5. Dark current at 55 degree C for pixels with different size. Solid curve shows reduction of dark current with scaling to pixel area

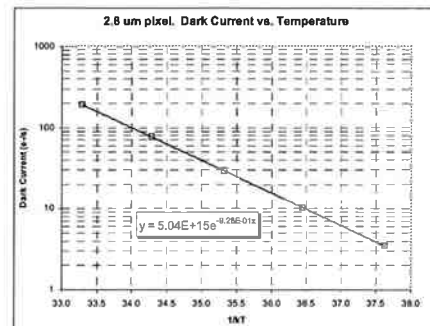
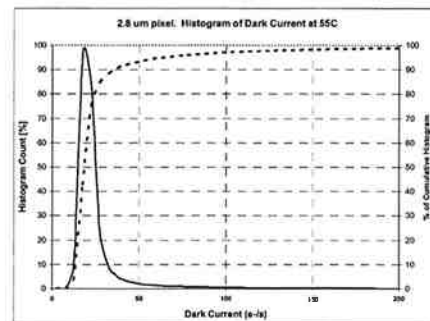


Figure 6. Dark current characteristics of 2.8 um pixel array at 55 C. a – histogram (solid line and left axis) and cumulative percent of distribution (dotted line and right axis); b – dark current vs. temperature

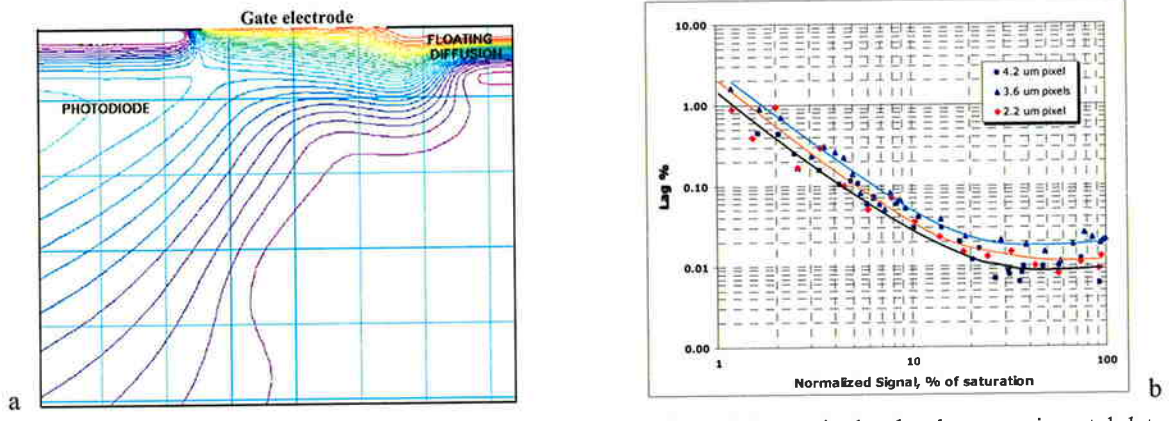


Figure 7. Lag of small pixels. a – simulation of potential profile for 2.8 um pixel; b – lag experimental data.

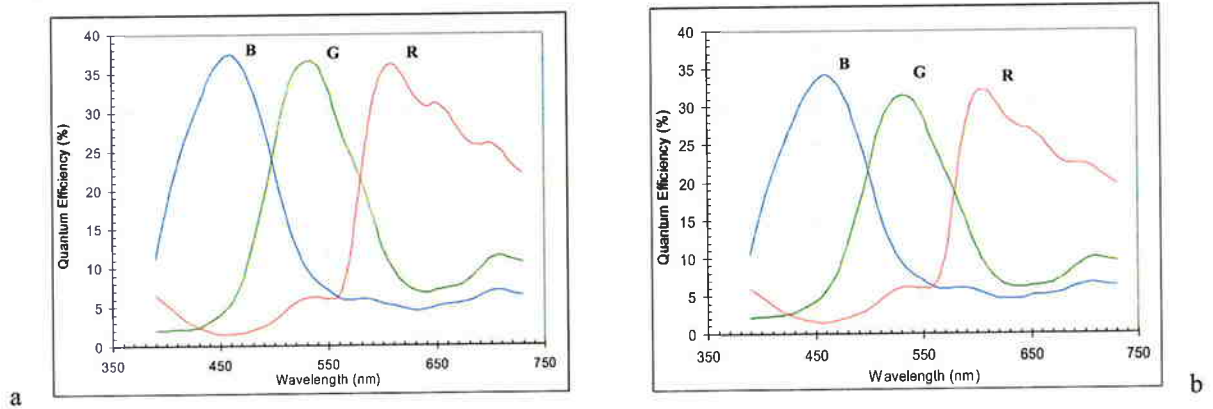


Figure 8. Spectral characteristics and crosstalk for 2.8um pixel array.

a – pixels at the center of the array, incident light  $f/2.8$ , CRA=0 degree. Crosstalk average: 18.4 %

b – pixels at the horizontal edge of the array, incident light  $f/2.8$ , CRA=20 degree. Crosstalk average: 20.9 %

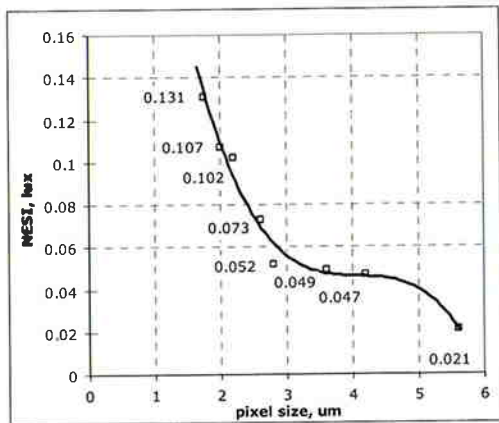


Figure 9. Noise equivalent scene illuminance for pixels with different size ( $f/2.8$ , 5 FPS)



Figure 10. Color Image from 900x640 pixel array with 1.7um pixel size

Table 1

	5.6-um	4.2-um	3.6-um	2.8-um	2.2-um	1.7 um
Responsivity (FD), V/(Lux*sec)	2.80	1.20	1.00	0.98	0.51	0.32
Quantum efficiency (G)	0.51	0.45	0.45	0.40	0.40	0.40
Pixel capacity (linear range), ke	30	26	26	17	12	9
SNR max, dB	44.7	44.1	44.1	42.3	40.7	39.5
Noise floor at max gain, e	8.0	8.8	7.0	3.8	3.6	2.8
Pixel dynamic range, dB	71.4	69.4	71.3	73.0	70.3	70.1
Dark current (55C), e/s	300	160	100	30	24	15
NESI ( $f/2.8$ , 5 FPS), lux	0.021	0.047	0.049	0.052	0.102	0.131