

The Tolerance for FD Dark Current and PD Overflow Current Characteristics of Wide Dynamic Range CMOS Image Sensor Using a Lateral Overflow Integration Capacitor

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Abstract

In a wide dynamic range (WDR) CMOS image sensor featuring a lateral overflow capacitor in a pixel, the tolerance for the floating diffusion (FD) dark current and the photodiode (PD) overflow current characteristics are discussed. The high tolerance for the FD dark current enables the simplified noise reduction approach to subtract the next filed noise (N_2') from the current filed signal (S_2+N_2) with no significant degradation of the image quality. It also leads to no need of the frame memory in the system. The PD overflow current characteristics based on the device simulation result in the overflow photoelectrons almost completely integrated at FD and the lateral overflow integration capacitor (CS) with the minimum substrate current.

Introduction

It is needless to say that the latest requirements for the image sensing devices are a high sensitivity, a high S/N ratio and a high resolution. In addition, a dynamic range enhancement which is comparable to the naked eye or the silver salt film camera is strongly required. The several recent papers have described the solution to the dynamic range enhancement. The conventional approaches, the multiple samplings in the divided exposure time [1-5] and the logarithm conversion method each pixel [6-7] have single or multiple issues in the moving image quality, S/N ratio and the image lag performance.

The novel wide dynamic range (WDR) CMOS image sensor featuring a lateral overflow capacitor in a pixel, which integrates the overflowed charges from a fully depleted photodiode during the exposure, has previously achieved a 100 dB dynamic range with keeping a high sensitivity and a high S/N ratio in low light to very bright light, without split of integration time [8].

In this paper, the tolerances for the FD dark current and the reset noise in the saturated overflow signal (S_2) of the WDR CMOS image sensor are evaluated. In order to keep the ideal linearity in S_2 , the saturated overflow photoelectrons have to be completely integrated at the floating diffusion (FD) and the lateral overflow capacitor (CS) without the leakage to the substrate. The photocurrent overflow characteristics are also discussed.

Fundamental Concept & Operation

Fig.1 shows a pixel schematic circuit diagram. The pixel circuit consists of a fully depleted photodiode (PD), a transfer switch (M1), a floating diffusion to convert the

charge to the voltage (FD), a reset switch (M2), a source follower amplifier (M4), a pixel select switch (M5), an overflow photoelectron integration capacitor (CS) and a switch between the floating diffusion FD and the overflow capacitor CS (M3). It is found that the new pixel circuit is just the addition of the overflow capacitor CS and the switch M3 to the conventional four transistors type CMOS image sensor.

The vertical or the lateral overflow drain operation which is widely used for the conventional CCD and CMOS image sensors loses the signal electrons overflowed from the photodiode. On the contrary, the new WDR CMOS image sensor is capable of integrating almost all the signal electrons at FD+CS. The switch M1 works as the suitable overflow path between PD and FD. The dynamic range is extended by fully utilizing all the generated photoelectrons at PD, regardless of the integration at PD or the overflow from PD.

Fig.2 shows the timing diagram of pixel operation. Prior to the exposure, the switch M3 and M5 are turned on and the other switch M1 and M2 are turned off. The photodiode PD is fully depleted at this moment. Then the switch M2 is turned on to reset both FD and CS. The reset noise including the M4 threshold voltage variation for the bright signal is read out as N_2 soon after turning the switch M2 off. During the exposure, the non-saturated photoelectrons are integrated at PD in the charge integration period. All the saturated overflow photoelectrons are also integrated at FD+CS through the M3. This operation enables the overflow photoelectrons to be utilized for the signal charges. After the integration, the switch M5 is turned on and the floating diffusion FD is reset by turning the switch M3 off and M2 on. The reset noise at FD including the M4 threshold voltage variation is read out as N_1 . The photoelectrons at PD are transferred to FD by turning switch M1 on. The signal S_1+N_1 is read out soon after turning the switch M1 off. Finally, all the charges are mixed at FD+CS by turning the switch M3 on and M1 on/off then the signal S_2+N_2 is read out.

Fig.3 shows the block diagram of the CMOS image sensor with the lateral overflow capacitor in a pixel. The signal and noise hold circuits are incorporated just next to image cell array. Four outputs are placed to read out the reset noise N_1 , S_1+N_1 , N_2 and S_2+N_2 . The off chip differential amplifier performs the subtraction of the noise component from the signal.

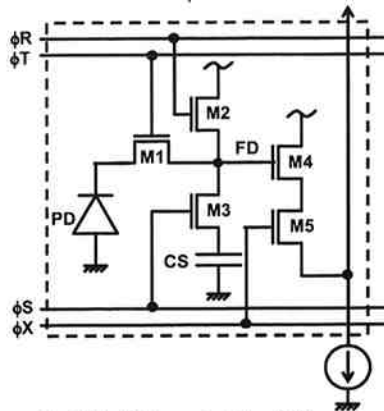


Fig.1 Pixel Schematic Circuit Diagram.

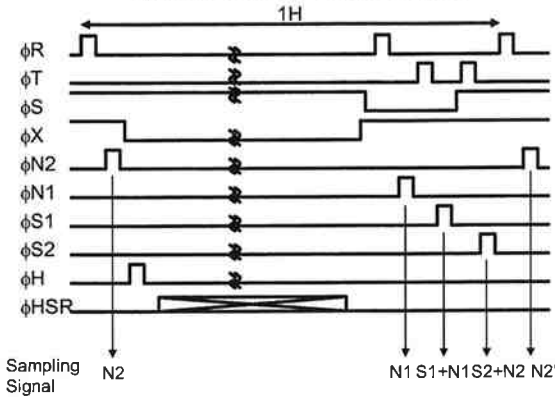


Fig.2 Timing Diagram of Pixel Operation.

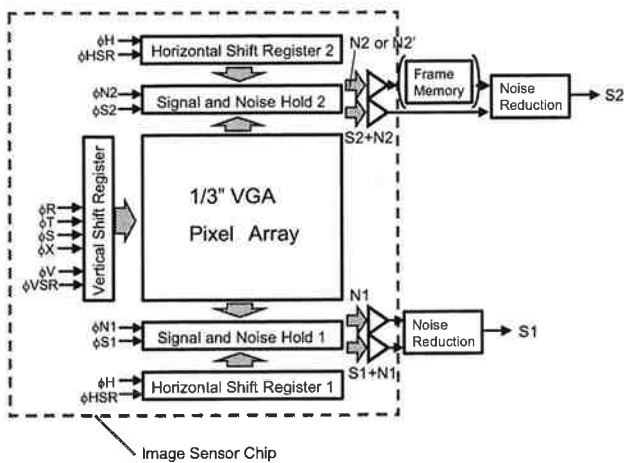


Fig.3 Block Diagram of the Image Sensor.

High Tolerance for FD Dark Current & PD Overflow Current Characteristics

In the basic operation of the sensor, the saturated overflow signal (S2) is selected when the non-saturated signal (S1) is close to the saturation. Since the signal S2 contains a relatively large number of the photoelectrons including the non-saturated and the saturated overflow photoelectrons, the high tolerances for the reset noise and the dark current are realized. The reset noise component of N2 is much smaller than that of N1 because the CS capacitance is much higher than the FD capacitance. By utilizing this characteristic, the simplified noise reduction approach to subtract the next field noise (N2'), instead of the current field noise (N2), from the current field signal (S2+N2) can be introduced. A high S/N ratio at S1/S2 switching point is achieved by the simplified noise reduction approach although the only fixed pattern

noise component is removed. It has also lead to no need of the frame memory in the system. The detailed S/N ratio estimation at S1/S2 switching point is discussed as follows.

The reference voltage (VSL) to switch the signal S1 to S2 is defined as close to the saturation voltage of S1. In the regular noise reduction approach with the frame memory, the S/N ratio (SNsl) of S2 at the S1/S2 switching point is derived by following equations.

$$SN_{sl} = VSL' / V_n \quad (1-1)$$

$$VSL' = VSL \cdot C_{FD} / (C_{FD} + C_{CS}) \quad (1-2)$$

$$V_n = Q_n / (C_{FD} + C_{CS}) \quad (1-3)$$

VSL: The reference voltage to switch the signal S1 to S2.

V_n: The residual noise voltage resulting from the same field noise reduction.

Q_n: The residual noise charge resulting from the same field noise reduction.

In the simplified noise reduction approach, the equations (1-1), (1-2) and (1-3) correspond to the below equations (2-1), (2-2) and (2-3), respectively.

$$SN_{sl} = VSL' / V_n' \quad (2-1)$$

$$VSL' = VSL \cdot C_{FD} / (C_{FD} + C_{CS}) \quad (2-2)$$

$$V_n' = Q_n' / (C_{FD} + C_{CS}) = \sqrt{(2kT(C_{FD} + C_{CS}) + Q_n'^2) / (C_{FD} + C_{CS})} \quad (2-3)$$

V_n': The residual noise voltage resulting from the next field noise reduction.

Q_n': The residual noise charge resulting from the next field noise reduction.

Fig.4 shows the relationship between the S1/S2 switching reference voltage (VSL) and the residual noise with various FD capacitances, in the case of keeping a benchmarked S/N ratio at 40 dB. The acceptable residual noise including the dark current shot noise in S2 is a rather high number of electrons. Assuming all the residual noise as the dark current shot noise, the tolerance for the dark current at FD+CS (I_{DARK}^{FD+CS}) is described as below equation.

$$I_{DARK}^{FD+CS} = qQ_n'^2 / (C_{FD} + C_{CS}) / t_{int} \quad (3)$$

q: unit charge

t_{int}: integration time

On the other hand, the tolerance for the dark current at PD (I_{DARK}^{PD}) is described as below equation.

$$I_{DARK}^{PD} = qQ_n^2 / t_{int} \quad (4)$$

Comparing the above equation (3) with (4), it is obvious that the tolerance for the dark current of FD+CS is higher than that of PD.

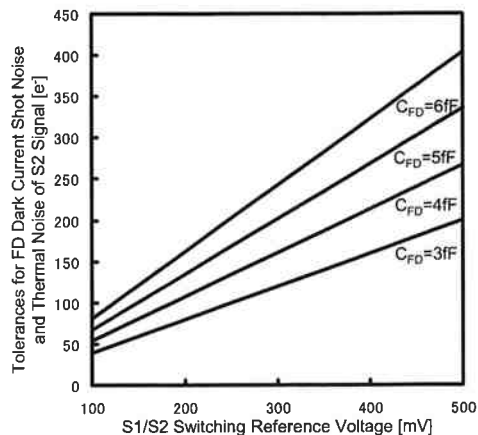


Fig.4 Tolerances for FD Dark Current Shot Noise and Thermal Noise in Signal S2.

In order to verify if the overflow photoelectrons are completely integrated at FD+CS, the device simulations have been performed. Fig.5 shows the schematic cross sectional view of the pixel and the extracted region for the device simulations. The device simulations result in the overflow characteristics of PD, as shown in Fig.6 and Fig.7. Fig.6(a) and Fig.7(a) show the current vector 2D plot diagram under the different incident light intensity. The lateral overflow current to FD and the substrate current are calculated by integrating the total current flux into FD junction and the substrate contact at $Z=3.0\mu\text{m}$, respectively. Fig.6(b) and Fig.7(b) correspond to the saturated S1/ the non-saturated S2 and the just saturated S2. For both cases, the ratio of the lateral overflow photocurrent (to FD+CS) to the substrate current is found to be high enough around 1000. The difference in potential barrier between the silicon surface under M1 and the Pwell below PD is about 0.32V. As a result, almost all the signal charges overflowed from PD have been integrated at FD+CS and it leads to an ideal linearity in the signal S2.

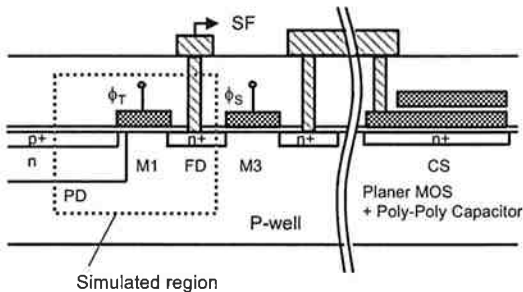


Fig.5 Schematic Cross Sectional View of the Pixel.

Image Sensing Performance

The 1/3" VGA format (640H x 480V pixels), $7.5 \times 7.5\mu\text{m}^2$ pixel CMOS image sensor with $6.6 \times 5.9\text{mm}^2$ chip size was fabricated through $0.35\mu\text{m}$ 2P3M CMOS process. The capacitance ratio of FD+CS to FD is about 16. In addition to the black & white sensor, the color sensor was also fabricated through RGB Bayer color filters and on-chip micro lenses process. The noise reduction was performed by the simplified approach to subtract the next field noise $N2'$, instead of the current field noise $N2$, from the current field signal $S2+N2$. Fig.8 shows the photo-electric conversion characteristics of the sensor. The dynamic range is extended to 102 dB by selecting either S1 or S2 signal, with ideal linear response from 0.015 lx and 1050 lx.

Fig. 9 shows the color sample images capturing the inside/outside of the room. Fig. 9(a), (b) and (c) correspond to the non-saturated signal S1, the saturated over flow signal S2 and the wide dynamic range signal, respectively. Fig. 9(a) and (b) are displayed as the upper 8 bit resolution by applying the gamma correction ($\gamma \approx 0.45$) to 12 bit resolution data after the A/D conversion. Fig. 9(c) is also displayed as 8 bit resolution for printing purpose by applying the gamma correction ($\gamma \approx 0.15$) to 16 bit resolution dynamic range image data. Even though the simplified noise reduction method without the frame memory is used, no specific noise is found in the region of switching the signal S1 to S2.

Fig.10 shows the black and white sample images capturing the flashlight and the incandescent lamps. The high tolerance for the blooming even in the bright spot light is demonstrated.

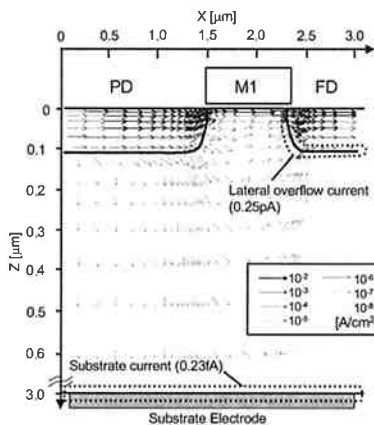


Fig.6(a) Current Vectors 2D Simulation.

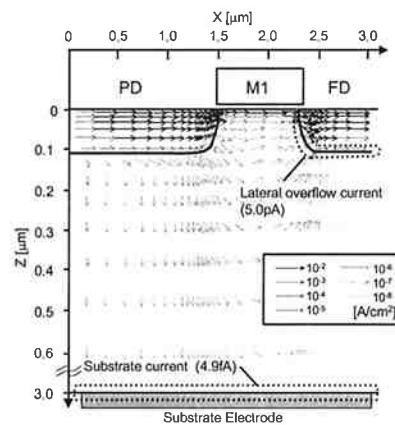


Fig.7(a) Current Vectors 2D Simulation.

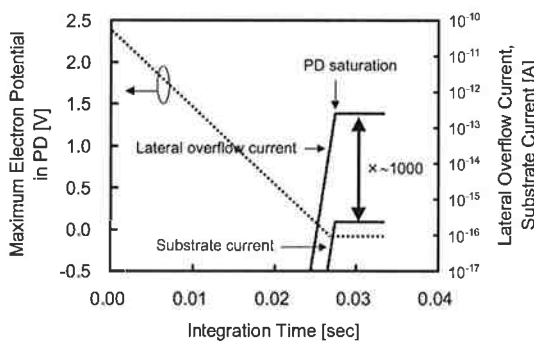


Fig.6(b) Maximum Electron Potential in PD and Lateral Overflow Current and Substrate Current as a Function of Integration Time.

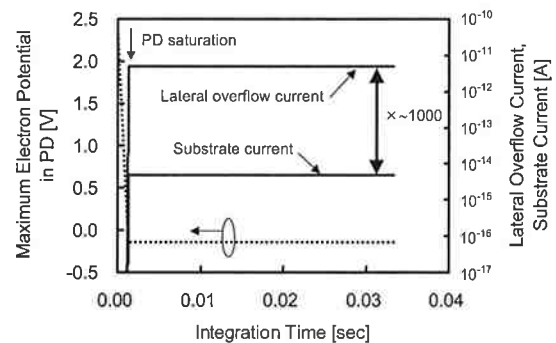


Fig.7(b) Maximum Electron Potential in PD and Lateral Overflow Current and Substrate Current as a Function of Integration Time.

Fig.11 shows the summary of the image sensor performance. The device performance results in a high sensitivity and a high S/N ratio with 0.15mVrms random noise and 0.15mVrms FPN. The calculated tolerance for the random noise in S2 is around 300 electrons. The dynamic range has reached 100 dB without image lag detection.

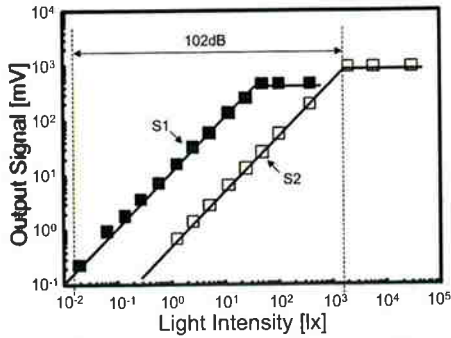


Fig.8 Photo-electric Conversion Characteristics.



Fig.9(a) Sample Image (S1).

Fig.9(b) Sample Image (S2).



Fig.9(c) Sample Image (WDR).

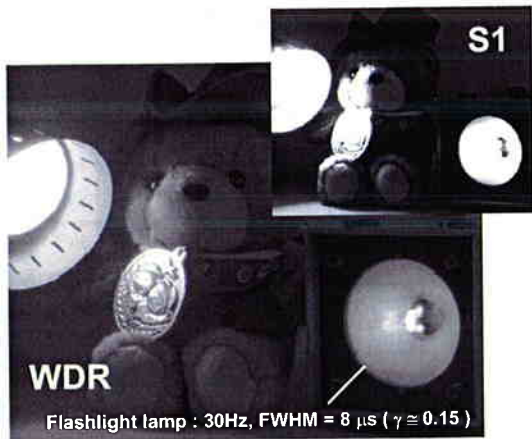


Fig.10 Picture of Flashlight and Incandescent Lamps (S1, WDR).

Process technology	0.35μm 2P3M CMOS
Optical format	1/3 inch
Pixel size	7.5 x 7.5 μm ²
Number of effective pixels	640 x 480
Supply voltage	5 V
Frame rate	30 fps
Random noise	0.15 mV _{rms}
FPN	0.15 mV _{rms}
Lag (S1, S2)	Under Detection Limit
Tolerances for FD dark current shot noise and reset noise	150e ⁻ - 300e ⁻ *
Saturation of S1	460 mV
Saturation of S2	950 mV
Effective saturation of S2 (saturation of S2 x 16)	15.2 V
Dynamic range	100 dB

* In the case of C_{FD}=3fF-6fF at S1/S2 switching reference voltage = 370mV.

Fig.11 Specification and Characteristics.

Conclusion

In a CMOS image sensor featuring a lateral overflow capacitor in a pixel, which integrates the overflowed charges from a fully depleted photodiode during the same exposure, a high S/N ratio has been realized by subtracting the next field noise component (N₂') from the current field signal (S₂+N₂'), without frame memory.

The ratio of the lateral overflow photocurrent (to FD+CS) to the substrate current from PD is found to be about 1000. It means almost all the signal charges overflowed from PD are integrated at FD+CS with the minimum leakage to the substrate. The novel WDR CMOS sensor realizes the high tolerances for the FD dark current shot noise and the reset noise with the ideal PD overflow characteristics.

References

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