# Fabrication and Initial Results for a Back-illuminated Monolithic APS in a mixed SOI/Bulk CMOS Technology

Bedabrata Pain
Jet Propulsion Laboratory
California Institute of Technology
4800 Oak Grove Drive, Pasadena, CA 91109
Phone: 818-354-8765; Fax: 818-393-0045; Email: bpain@jpl.nasa.gov

The thickness of metals and inter-level dielectric (ILD) layers does not scale with the reduction of CMOS feature size. As a result, the pixel aspect ratio (i.e. the ratio of the pixel height to its pitch) of a CMOS imager increases rapidly as the pixel pitch is reduced. The increase of aspect ratio causes enhanced optical cross-talk, reduced photo-response, and poor angular response [1]. In addition, a front-illuminated imager also suffers from obscurations from the metal lines crisscrossing the pixel area. To solve these problems, ILDs with complex air-guard structures [2] and thinner ILDs with copper metallization and low-k dielectrics [3] are being developed. Another approach is to operate the imager with back-illumination. With back-illumination, ILD and metal-line related effects are eliminated, and the imager can operate with near 100% fill-factor. Thus, a back-illuminated CMOS imager is expected to provide a number of advantages, such as high quantum efficiency, excellent angular response, availability of additional space in the pixel for integration of in-pixel processing circuits, efficient implementation of anti-reflection coatings, and compatibility with the next generation copper technology and low-k dielectrics.

In order to operate an imager in a back-illuminated fashion, the imager substrate needs to be thinned. After thinning, the interface trap density at the unterminated silicon surface is unacceptably high, while a naturally formed native oxide (~20 °A thickness) causes the surface to become positively charged. Unwanted band-bending and the presence of dangling bonds result in a loss of short-wavelength quantum efficiency (QE) and abnormally high dark currents, necessitating the use of post-metallization surface-passivation steps [4].

A manufacturable thinning process must be carried out at wafer level and must address the problems of having of excellent surface planarity and post-thinning surface passivation. Figure 1 shows the conventional thinning approach, as has been applied to CCDs. This approach highlights the difficulties related to etch stop and surface-passivation. High temperature processing (inherent in micro-fabrication) tends to blur the boundary between the heavily doped substrate and epitaxial silicon. In turn, the absence of a sharp boundary between the substrate and epitaxial silicon causes difficulties for uniform thinning. Moreover, post-metallization surface passivation is difficult, since high temperature anneal is ruled out. Novel passivation techniques such as UV-flooding, flash gates, pulsed-laser anneal, low-pressure oxide deposition, and MBE-based delta-doping are either difficult to integrate with a CMOS process flow or unstable [5,6,7,8,9]. Other backside imager implementation techniques involve the use of wafer-bonding and 3D integration [10] or bump-bonding [11], neither of which are part of the mainstream VLSI technology at this time.

We have developed a manufacturable wafer-level thinning process that solves the above-mentioned problems. Figure 2 shows the process and the schematic cross-section of our back-illuminated CMOS imager that uses a SOI wafer. The starting wafer consists of a thermal oxide buried between a low-doped thick p-type silicon wafer, and a p-type device silicon with appropriate thickness and doping (e.g. 5 µm thick and $2x10^{14}/cm^3$ boron doping). The thick silicon wafer is used as handle-wafer for mechanical support. The imager was implemented on the device silicon using a conventional bulk-CMOS process flow. Step 2 shows the schematic cross-section after CMOS device fabrication. Prior to thinning, the structure is bonded to a glass wafer for mechanical support, as shown in step 3. Note that glass wafer bonding is not critical – any organic material will work just as well. The silicon handle-wafer is then removed through a combination of grinding and wet etching (e.g. hot-KOH followed by TMAH) (step 4). In this case, the buried $SiO_2$ provides a natural etch stop, generating a uniformly planar back surface where light will be eventually collected. In addition, the resultant structure is self-passivated since it consists of thermally grown

$Si-SiO_2$ interface. A PECVD nitride is deposited for simultaneously minimizing reflection and providing additional passivation of the remaining dangling bonds.

We have designed and fabricated a collection of imager pixels with source-follower readout and area and perimeter diodes both on the SOI wafers and bulk wafers using a 0.5 μm LOCOS-based bulk-CMOS process. The pixels were implemented in a 3x3 array, with the central-pixel of the cluster being read out. The bulk wafers were not thinned. The SOI wafers were covered with nitride after thinning, and subjected to $H_2$ anneal.

Proof-of-concept operation was demonstrated by illuminating light on both front and back-illuminated pixel types. The pixels and the diodes responded to light, and produced output in a manner similar to that of a good imaging pixel. The operation was verified by measuring the mean-variance curve under illuminated condition. Figure 3 shows the measured mean-variance curve from the back-illuminated pixels implemented in the new process, indicating proof-of-concept pixel operation. Figure 4 shows that with back-illumination the QE increased to ~ 80%, even though the anti-reflection coating was far from optimum. Since only one metal layer was used, the front-illuminated imager also produced reasonably high QE that will not be the case for an actual imager with smaller pixel size and multi-level metal.

In conclusion, we have demonstrated a manufacturable back-illuminated imager fabrication technology and architecture, and obtained initial results to demonstrate the viability of the approach. Additional work relating to the development of large format imagers, backside pad connections, and microlens deposition is under way.

**Acknowledgments:**

The assistances of Prof. D. Misra of NJIT, Dr. M. Tischler of OSIS, Dr. T. Cunningham and Dr. S. Sesadri of JPL for fabrication support and critical comments are gratefully acknowledged. This research was carried out at the Jet Propulsion Laboratory, California Institute of Technology, and was sponsored by United States Space Missile Command and United States Missile Defense Agency through an agreement with the National Aeronautics and Space Administration.

**References:**

1. G. Agranov et al., *IEEE Trans. Electron Devices,* vol. 50, pp. 4-11, 2003
2. T.H. Hsu et al., *IEEE Electron Device Lett.*, vol. 25, pp. 375-377, 2004
3. J.W. Adkisson et al, *IEEE Workshop on charge coupled devices and advanced image sensors*, 2005
4. S. Nikzad et al., *Proc. SPIE*, vol. 2198, pp. 907, 1994
5. R. A. Stern, *Proc. SPIE*, vol. 1071, pp. 43–57, 1989
6. M. Lesser, *Proc. SPIE,* vol. 1447, pp. 177-183, 1991
7. P.A. Levine, *Proc. SPIE*, vol. 2172, pp. 100–114, 1994
8. B.E. Burke et al., *Tec. Dig. 1998 IEEE Intl. Elec. Dev. Meet*, pp. 33-36, 1998
9. J.R. Tower et al., *IEEE Trans. Electron Devices,* vol. 50, pp. 218-224, 2003
10. V. Suntharalingam et al., *Tec. Dig. 2005 IEEE Intl. Solid-state Circ. Conf.*, pp. 356-357, 2005
11. Y. Bai et al., *Proc. SPIE*, vol. 5167, pp. 83-93, 2004

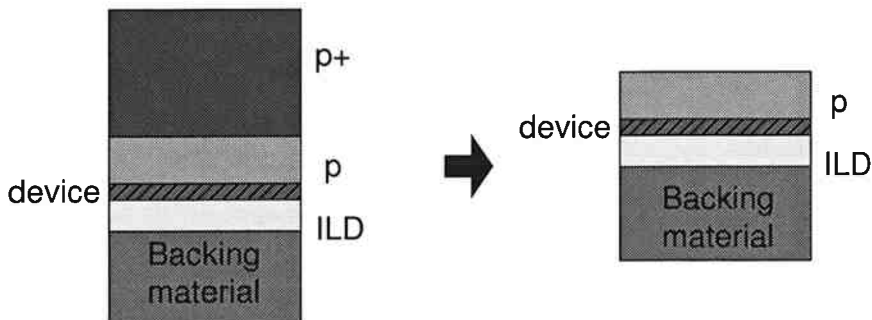


**Figure 1: Traditional thinning as applied to CCDs**

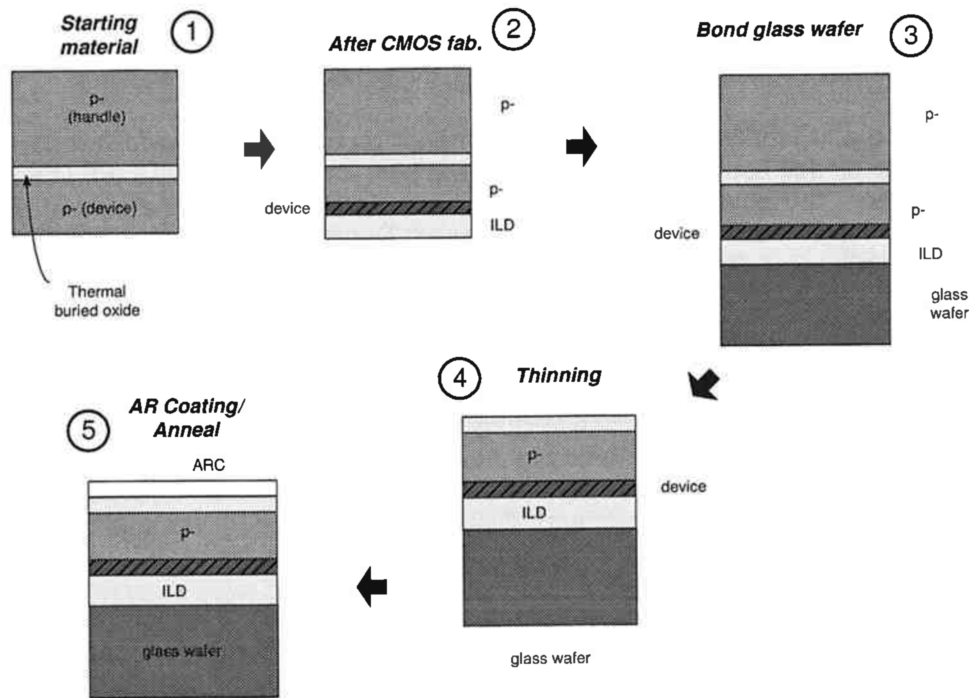


Figure 2: Process flow and cross-section of the structure for back-illuminated CMOS imager implementation

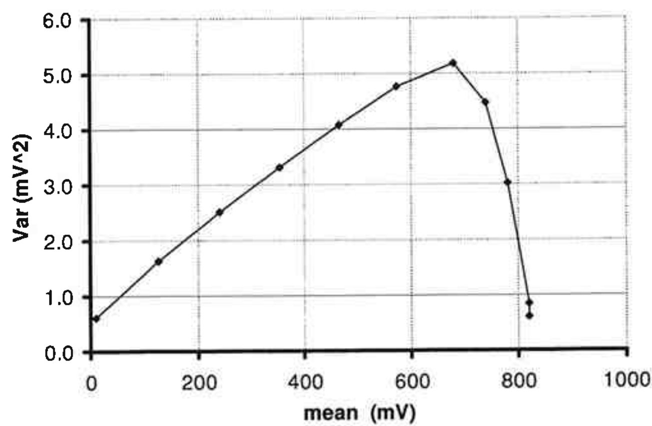


Figure 3: Measured mean-variance curve of a an individual pixel

Figure 4: Measured quantum efficiency for back and front-illuminated pixels