

High-end CMOS Active Pixel Sensor for Hyperspectral Imaging

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Abstract

Solid-state optical sensors are used in the space environment for a wide range of applications. Many applications still rely on charge coupled device (CCD) technology, but CMOS active pixel sensors (APS) offer great promise for use in space-borne imaging instruments. This paper highlights an ongoing development under ESA contract for a high-end CMOS APS sensor optimized for hyperspectral imaging in space [1].

1. Introduction

In recent years, many developments were started to investigate how CMOS APS could replace CCDs in several low to medium end space imaging applications (e.g. attitude and orbit control systems). These developments were driven by the idea that those applications could cash-in on CMOS APS's inherent advantages over CCDs like on-chip functionality, low power operation, high speed, fast technological progress, windowed readout for simultaneous tracking of objects, better radiation tolerance due to the lack of CCD-like transfer loss, etc. It was expected for a long time that high-quality scientific imaging would remain out of reach for CMOS sensors since they lacked the required performance in noise, non-uniformity and dark signal levels. Hence they could not compete with high-end scientific CCDs that offer high quantum efficiency, large dynamic range and special operation modes as Time Delay Integration (TDI) and binning.

2. Application

In this paper we present the development of a CMOS imager that aims to achieve CCD-like performance required for hyperspectral earth and planetary observation while adding above-mentioned CMOS advantages. The goal of such space missions is to observe parameters encompassing agriculture, forestry, soil/geological environments and coastal zones/inland waters. These data can be used to improve our understanding of geospheric processes. Figure 1 illustrates the principle of hyperspectral imaging. The sensor consists of a 2-D pixel array. While the satellite moves with respect to the earth, the sensor's x-axis is used to retrieve the spatial information of a ground line

represented by the spectrometer slit. The second dimension (y-axis) is used for the reproduction of the spectral information. The resulting image data together with the track of the satellite will then constitute the so-called image cube.

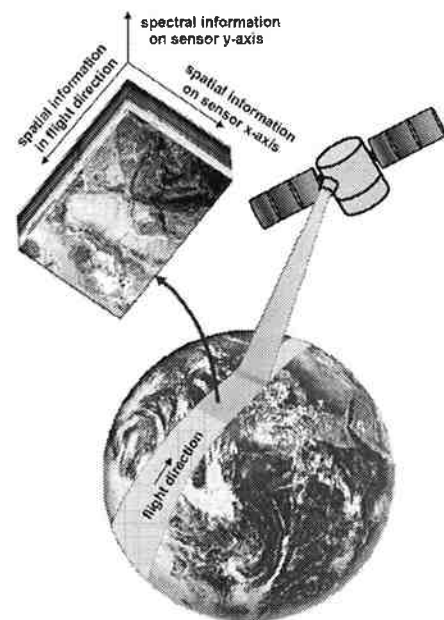


Figure 1. Principle of spaceborne hyperspectral imaging.

Important requirements for the sensor are snapshot operation to avoid image distortion due to the satellite's movement and high frame rates, combined with large full well charges, low noise and high quantum efficiency.

3. Sensor description

Figure 2 shows the architecture of the readout sensor. The pixel pitch is 22.5 μm in both X and Y direction. Since the size of the device is larger than the reticle size, the sensor requires the stitching technique in which smaller blocks are repeated on the wafer. The pixel array consists of stitch blocks of 512 by 512 pixels and is stitchable up to 2048 by 2048 pixels. Hence, the resolution of the pixel array is not fixed. Columns are multiplexed in groups of 256 to a pseudo differential output (signal and reference output). Each output runs at a maximum readout frequency of 20 Mpixels/s.

The serial-to-parallel interface (SPI) allows to program the Y start address and X start addresses for each column block individually. The offset and gain of each output

can be modified independently as well or outputs can be put in standby mode. The sensor has also a non-destructive readout operation mode. The whole sensor is designed using proprietary techniques to achieve high radiation tolerance [2][3].

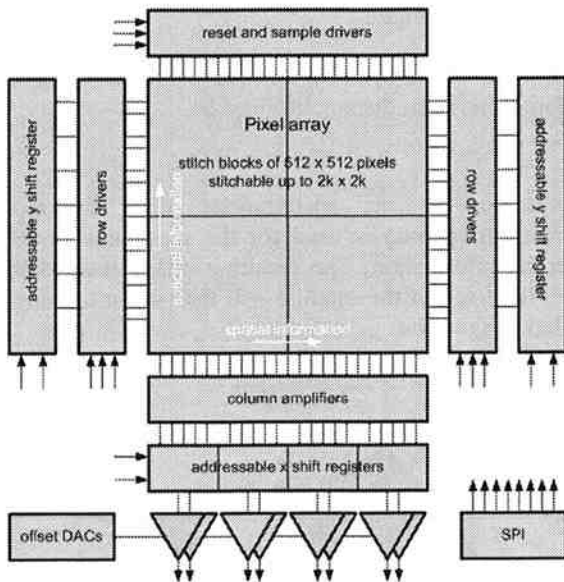


Figure 2. Sensor architecture.

The readout sensor as shown in Figure 2 is implemented for the use in a hybrid approach but has also the option to be used as a monolithic, backside thinned, backside illuminated image sensor on its own (Figure 3(b)).

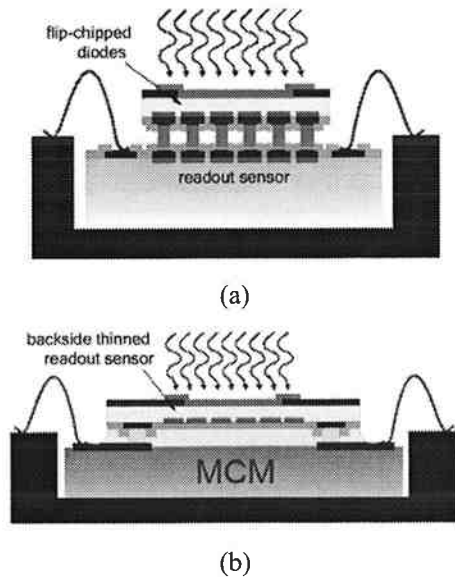


Figure 3. Hybrid approach (a) or monolithic backside illuminated sensor (b).

In the hybrid approach, the readout circuit is combined with hybrid Si diodes processed on wafers that are afterwards thinned, diced and flip-chipped on the readout sensor using 10 μm Indium bump technology (Figure 3(a)).

The pixel consists out of two stages: a light detecting stage and a sample and hold stage with three storage capacitors. This architecture, as shown in Figure 4,

allows for a true pipelined synchronous shutter with on-chip correlated double sampling (CDS), i.e. all pixels start and stop integration at the same moment while the previous frame is still read out.

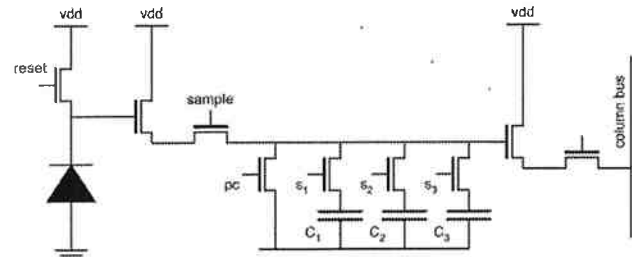


Figure 4. Snapshot shutter pixel with 3 storage capacitors.

The main pixel characteristics are given in Table 1. The pixel readout noise is determined by the size of the storage capacitors. The three capacitors, made by poly on diffusion, occupy about 70 % of the pixel area and equal each 350 fF. The photodiode capacitance is about 15 fF in case of the monolithic sensor and can vary from 25 fF to more than 1 pF in the hybrid approach.

Table 1. Pixel design characteristics.

	monolithic	hybrid
in-pixel storage capacitance (fF)	350	350
full well charge (x 1000 electrons) (FWC)	150 - 200	250 - 1000
read noise (electrons)	15 - 20	25 - 100
dynamic range (FWC/dark noise) (dB)	80	80
maximum SNR	388-447	500 - 1000

This pixel allows for different operations of readout to cope with a large dynamic range. Some are briefly discussed in the following subsections.

3.1 Normal readout

The basic operation of the imager consists of sampling the reset value of the pixel on capacitor C_1 , and the signal value after exposure on C_2 . After sampling of the signal value on C_2 , the readout of both capacitors can start (on a row by row basis). During readout, integration of the next frame can start by sampling the reset value of the pixel on capacitor C_3 . The third capacitance is required since at the start of the new integration period, the values on C_1 are not yet readout (at least not for all rows). Reset values are thus stored by toggling between C_1 and C_3 . Signal values are always sampled on C_2 . The final signal at the output is the voltage difference between C_1 and C_2 or C_3 and C_2 . Figure 5 illustrates the normal readout operation mode. Integration and readout time are independent. Readout of the frame happens immediately after integration of the frame and has a fixed length. The readout time is approximately 37 ms for the 2k x 2k sensor. It scales more or less linearly with the number of pixels in the Y direction of the sensor.

The sensor has a global shutter operation, i.e. the reset and sample signals from Figure 4 are global signals that are effective on all pixels in parallel. In the normal mode

of operation, the s_1 , s_2 , s_3 and pc signals are global during the reset and sample phase, but pulsed line by line during readout. Indeed, the sensor operates line-wise during readout: a line of pixels can be selected for readout into the column amplifier structures. Image acquisition is done by sequencing over all lines of interest and applying the required readout control to each line selected.

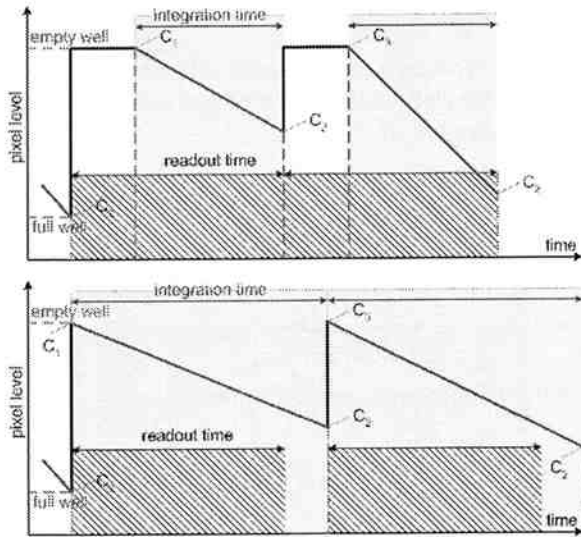


Figure 5. Normal readout: $T_{int} < T_{read}$ (top), $T_{int} > T_{read}$ (bottom).

3.2 Non-destructive readout (NDR)

The default mode of operation is with on-chip FPN correction (correlated double sampling and subtraction on-chip). However, the sensor can also be programmed to read out the pixels non-destructively. This mode of operation is shown in Figure 6.

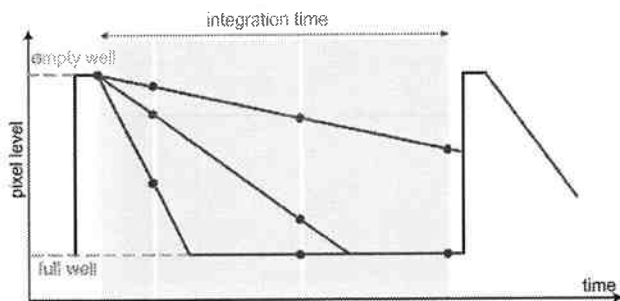


Figure 6. Principle of non-destructive readout.

After a pixel is initially reset, it can be read multiple times, without resetting. The initial reset level and all intermediate signals can be recorded. High light levels will saturate the pixels quickly, but a useful signal is obtained from the early samples. For low light levels, one has to use the later or latest samples. Since the pixel contains three storage capacitors, the time between consecutive samples is not limited by the readout time.

3.3 Normal readout with high dynamic range

With the implemented pixel architecture, it is also possible to increase the dynamic range in case the large dynamic range is only required between the rows and not

within the rows. As with NDR, it is possible to sample the pixel signals after a short exposure time and afterwards again without reset in between. For example, the reset values are sampled on capacitor C_1 . After a short integration period T_1 , the signals are sampled on C_3 . Finally, after the longer integration period T_2 , the signals are sampled on C_2 . Bright rows are read out using the pixel values from C_1 and C_3 and have a short integration time T_1 . Rows with low level illumination are read out using the pixel values from C_1 and C_2 and have a long integration time T_2 . The dynamic range thereby increases with the ratio of the integration times T_2/T_1 (pixel information not only resides in the voltage level but in the integration time as well).

The drawback of this readout sequence is that simultaneous integration of charges and readout of the previous frame is not fully guaranteed since the C_3 capacitors in the pixels also store signal information. However, this can be minimized by clever readout, e.g. first readout of the pixels with short integration time.

3.4 Normal readout with line by line variable integration time

Although the sensor normally operates as a synchronous shutter device, meaning that the integration starts and stops for all pixels at the same moment in time, the pixel architecture allows enough flexibility for the user to define a different integration time for each line individually. In this readout mode, the reset values of all pixels are sampled in parallel, i.e. all pixels are reset and their values are sampled on C_1 immediately afterwards.

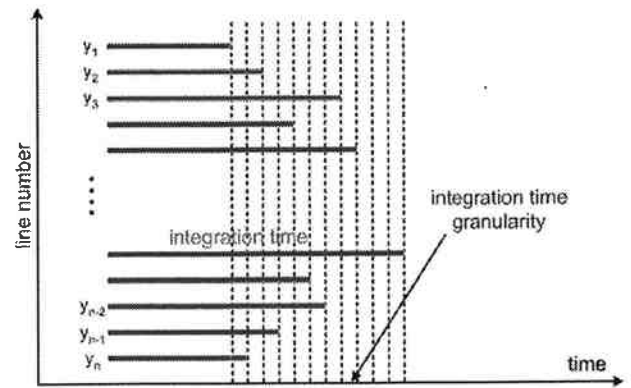


Figure 7. Readout with line by line variable integration time.

This is schematically shown in Figure 7. To sample the photodiode voltage at a certain time, both sample and s_x of the appropriate capacitor needs to be pulsed (see Figure 4). The sample line is a global line and can therefore not be controlled for each line differently. However, the s_x lines are either global or line-based, under user control.

Inherently to this architecture, each line will have a different integration time (unless a number of lines with the smallest integration time are sampled globally). The granularity of the integration time is limited by the upload of new Y address and initialization of the shift

register, sampling of the signals, and in case of read out of a previous frame certain timing restrictions on readout signals. The minimum granularity ranges therefore from a few microseconds to a few tens of microseconds.

3.5 Optimized pixel capacitance for hyperspectral imaging

The previous readout schemes alleviate the problem of a high dynamic range. However, they cannot solve the need for a very large shot noise limited signal-to-noise ratio (SNR) at certain wavelengths. In hyperspectral imaging a large full well is required to achieve the highest possible SNR in bright objects (e.g. clouds) in a particular wavelength range. On the other hand, a very low background noise is desirable for imaging of dim objects. Hence the need for a large full well and very low noise level. Typically, the two situations do not always occur in the same wavelength range (e.g. lowest background noise required at lower wavelengths, highest full well at longer wavelengths). The hybrid approach allows us to optimize the pixel capacitance depending on the wavelength, i.e. vary the pixel capacitance along the Y direction in the image array. This optimization can be obtained from the spectral response of the array and the expected spectral dynamic range of the irradiance. This is schematically depicted in Figure 8.

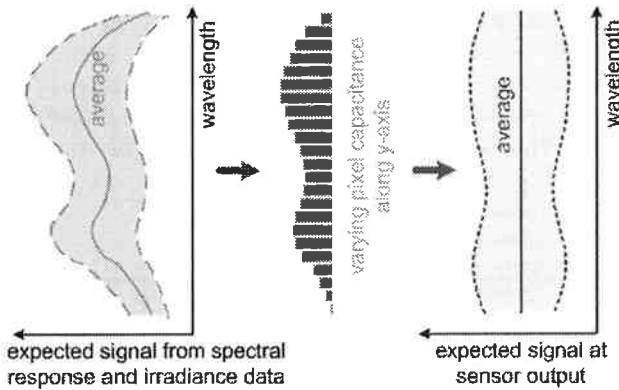


Figure 8. Hyperspectral imager with varying and optimized pixel capacitance along the vertical direction.

The optimization is based on the fact that one should try to amplify the pixel signal as soon as possible in the readout chain. The first stage is the pixel capacitance. This can further also be done in the gain stage at the output, which can be varied also from line to line.

4. Technology

The readout devices have recently finished processing in 0.35 μm XFAB technology, the diode arrays for hybridization were processed at Imec. Figure 9 shows a picture of a wafer with readout devices of different size and corresponding diode arrays.

At the end, both the hybrid detector and the monolithic sensor will be processed on custom 50 μm thick epitaxial wafers which results in enhanced quantum efficiency for longer wavelengths (NIR). The thick epi wafers have a

stepwise doping profile that will accelerate the collection of photo-generated charges and improve MTF [4]-[6].

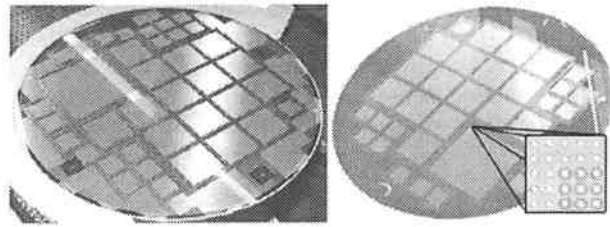


Figure 9. Processed XFAB wafer with readout devices of varying size (left) and matching Imec wafer with diodes for hybridization (right).

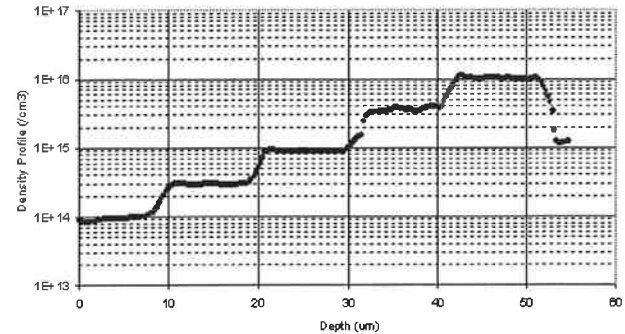


Figure 10. Measured doping profile of the 50 μm thick epi using Scanning Resistance Probing (SRP).

First functional tests have been started recently at Cypress/FillFactory on a 512 x 512 readout device (no flip-chip of hybrid diodes yet). The first image, taken with front-side illumination, is shown in Figure 11.

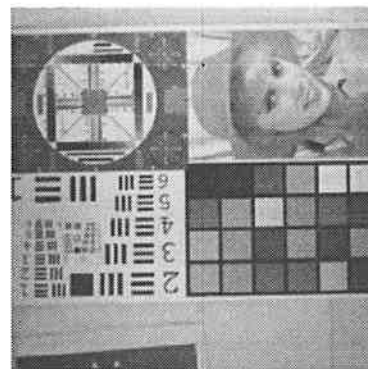


Figure 11. First image of 512 x 512 readout device (a cluster defect results in one single bad column and row).

Imec is currently working on the optimization of several post-processing steps like backside thinning (both for hybrid diodes as for readout devices), backside passivation, anti-reflective coating optimized for a broad wavelength range and techniques for cross talk reduction.

5. Conclusions

In this paper we presented the design of a CMOS image sensor for spaceborne hyperspectral imaging applications. The pixel is characterized by the implementation of three storage capacitors, which allow

for a synchronous pipelined shutter operation, combined with CDS on-chip. The sensor can be used either as readout chip for hybridized diodes or as monolithic backside illuminated device. Different readout schemes or line-wise optimization of the hybrid photodiode capacitances enable high dynamic range imaging required for this application. First device characterization tests are currently ongoing, as well as post-processing steps for hybridization and backside thinning.

References

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