

Optimization of Cu Interconnect Layers for 2.7 μm Pixel Image Sensor Technology: Fabrication, Modeling, and Optical Results

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Introduction

Many integrated circuit fabricators adopted copper metallization technology at the 180 nm or 130 nm nodes. The drive to use copper came from its lower resistivity and improved electromigration resistance compared to aluminum. For the same resistance and electromigration susceptibility, the metal thickness could be made thinner, reducing the line-to-line capacitance. For these technologies, the RC product was critical. Copper's susceptibility to oxidation, however, led to unique challenges and specialized fabrication techniques.

For image sensors, copper interconnection technology again confers significant advantages. By reducing the metal thickness, designers can take advantage of the reduced line-line coupling for noise reduction. The pixel performance is improved in two ways by the use of copper interconnects. First, Cu interconnect technology improves optical-path uniformity by reducing the polishing of the interconnect dielectric.¹ Second, the reduction in metal thickness for any given resistance or electromigration requirement allows shortening of the optical path. As pixel size is reduced, the optical stack height critically determines the angle response of the detector. However, just as for high performance applications, introduction of Cu interconnects for an image sensor leads to unique challenges and specialized fabrication.

Copper Fabrication Process

The copper fabrication process and resultant structure differs from aluminum in ways that impact image sensor performance. A simplified, single metal-layer schematic fabrication scheme is shown in Fig. 1. The subtractive aluminum process masks and etches the aluminum line on top of a dielectric. A gapfill dielectric, typically oxide, is then deposited and planarized. The copper process, instead, etches a trough in the dielectric, deposits a

protective liner, and then deposits copper. The copper is planarized, and nitride is deposited on top of the copper.

Cu Fabrication and Image Sensor Performance

The fabrication differences between aluminum and copper lead to changes in optical properties. First, in the case of aluminum, the oxide level is polished a considerable amount. At a minimum – the height of the aluminum layer is typically 350 nm. To reach the same final thickness of oxide, the deposition must be larger by the amount of polish. For the copper fabrication process, the oxide is typically only removed during the liner polish process, removing less than 100 nm. The subtractive aluminum image sensor process, therefore, suffers from thickness non-uniformity associated with both the additional oxide deposition and additional oxide polish.²

This oxide non-uniformity will cause uncertainty in the focal point of the microlenses, degrading the color and overall response of pixels, particularly in the corners of the microlenses. The polish is particularly sensitive in the corners of the array, where the uniform pattern density of the image sensor changes suddenly at the pixel/support boundary.

The nitride layer, shown in Fig. 1, for the copper fabrication scheme must be present in order to prevent the Cu from oxidizing during processing.³ If the nitride protective layer is omitted or compromised, electromigration degrades, or in the worst case, significant Cu oxides can be formed lead to severe morphology and performance problems. Exposure to plasma etching, resist strip – or even heating for extended periods – with water in the oxides, can degrade the copper lines. Use of Si_3N_4 is, therefore, convenient because it can serve as an effective etch stop as well as a stable oxidation barrier.

The $\text{SiO}_2 / \text{Si}_3\text{N}_4 / \text{SiO}_2$ structure, however, introduces a discontinuity in the refractive index as the light travels to the detection area. Reflections from these layers degrade the spectral response. Figure 2 shows the simulated optical response with and without the passivating silicon nitride layers. With the nitrides present, the reflectance can reach 60% at some wavelengths. The thicknesses of the oxide and nitride dielectric layers are subject to manufacturing tolerances, and these tolerances are a significant fraction of the wavelength of light in the dielectric. These reflections cannot be corrected because of the inherent variability in the manufacturing process.

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The passivating nitrides must be removed from the optical path in order to have acceptable optical performance. A number of methods are available to eliminate the nitride-induced reflections. The simplest approach preserves the nitrides over the copper layers but uses a mask to eliminate them in the optical path. An SEM showing the result is shown in Fig. 3. The nitrides are removed at each layer, in this case, with the same mask for each layer. The nitride is visible as a light band above the copper at metal 1, metal 2, and again, above the metal 3 dielectric. (No metal 3 is visible in this picture).

The experimental quantum efficiency from two pixel arrays without microlenses or color filters, one with the nitrides left in place, the other with the nitrides removed as in the SEM cross-section, are shown in Fig. 4. The results from the wafer with the nitrides still in place show degraded quantum efficiency at a number of wavelengths, in particular, near 520 nm, 590 nm, and 650 nm. The wafer with the nitrides removed shows no similar broad structure.

The masked method of removing the nitrides, while solving the reflectance problem, has obvious issues. First, the overlay tolerance makes the size of the nitride holes adequate, but smaller than desired, since the copper can in no instance be exposed to the nitride etch. Second, the process adds mask and etch steps, so it is costly and adds potential defect sources.

A more cost-effective solution is to use a self-aligned deposition of a barrier metal to protect the copper features. CoWP can be selectively deposited on the Cu features using an electroless plating technique after the copper polish. An SEM showing the CoWP deposition on the M2 copper line is shown in Fig. 5. CoWP layers effectively passivate the Cu surfaces, as measured by electromigration,⁴ as well as via resistance distributions and stress migration lifetime.⁵

Copper Stack Height and Experimental Results

The most significant advantage of Cu wiring in an image sensor is the reduction of the stack height. The relative comparisons of three different metallization technologies are shown in Fig. 6. The first diagram shows an aluminum metallization stack, the second shows a standard copper metallization, and the third shows an optimized copper process. We chose the reference aluminum thickness to provide equivalent resistance to the Cu metallization stack. For a four-level metal wiring process, three of which are active in the pixel area, the aluminum stack height is more than 30% thicker

than Cu. While the Al stack height can be reduced for an optimized image sensor technology to take advantage of the reduced resistance requirements relative to high performance logic,⁶ so too can the Cu stack be reduced. Using these BEOL options, we modeled the angle response of a representative 2.7 μm pixel, as shown in Fig. 7. Using 70% of the maximum response as the cutoff, the standard aluminum and copper metallization processes achieved 17 and 21 degrees angle response, as summarized in Fig. 8. Further shrinking the Cu BEOL stack to 2.1 μm above the height of the silicon improved the angle response further to 25 degrees.

We fabricated a 4 MP imager with 2.7 μm pixels in a four-transistor architecture using the standard Cu interconnect process, as shown in the center diagram of Fig. 6. Angle response, as shown in Fig. 9, is ± 20 degrees, although the response is miscentered by 2 degrees. The mis-centering of the lens is on the order of 50 nm relative to the photodiode, which is within our current alignment tolerances. The angle response in the perpendicular direction is reduced by the asymmetry of the photodiode design and the presence of the transfer gate within the photodiode. The angle response in the short direction of the photodiode is shown in Fig. 10. Simulations of the angle response, in Fig. 11, agree with the experimental results but again with an offset.

Beyond the Cu interconnect stack-height reduction, we optimized barrier nitride layers on top of the pixel to serve as an anti-reflection coating for blue response⁷ (see Fig. 3). In addition, we used a p-type layer to passivate the surface of the photodetector. The results of this optimization are shown in Fig. 12. Both the blue and red quantum efficiencies continue to be improved by a combination of silicon processing and lens optimizations.

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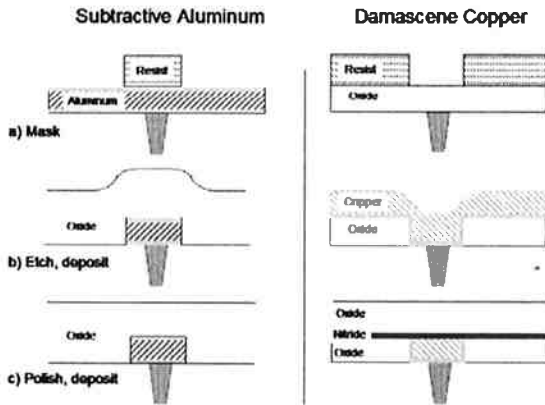


Fig. 1: Schematic fabrication scheme for aluminum and copper metallization.

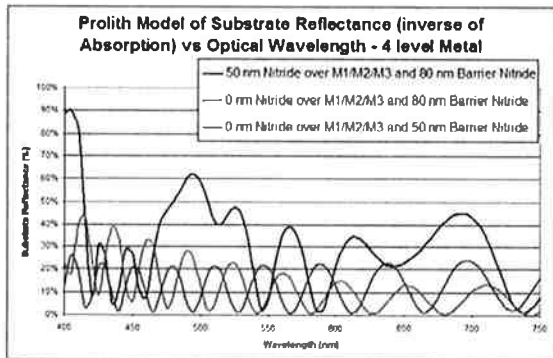


Fig. 2: Simulated reflectance of nitride films in the optical path. High reflectance present with interconnect-interlevel nitride dielectrics.



Fig. 3: Cross section of interconnect stack with nitrides removed in the optical path.

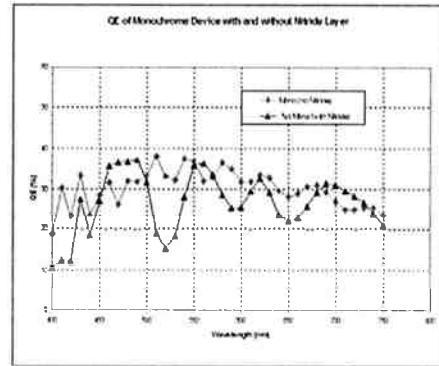
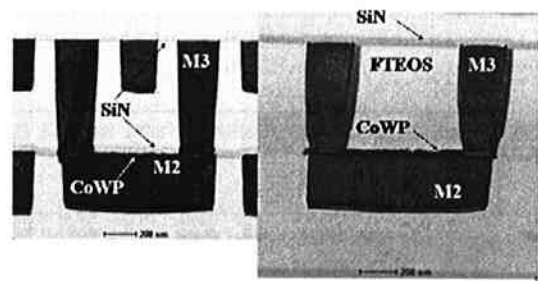


Fig. 4: Experimental quantum efficiency vs. wavelength response with and without nitride removal for an image sensor without color filters or microlenses.



a) 20 nm CoWP + 50 nm SiN b) 40nm CoWP ; no SiN cap

Fig. 5: Comparison of passivation with a) nitride or with b) CoWP selective deposition.

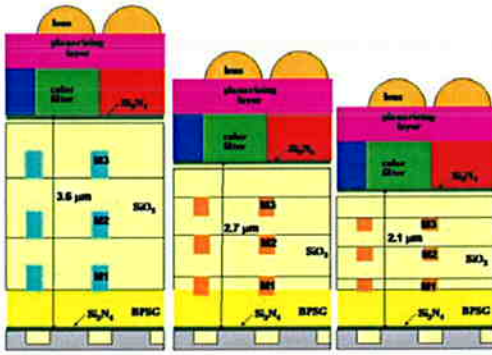


Fig. 6: Schematic drawing comparing thicknesses for logic-compatible aluminum, copper, and an optimized copper interconnect technologies.

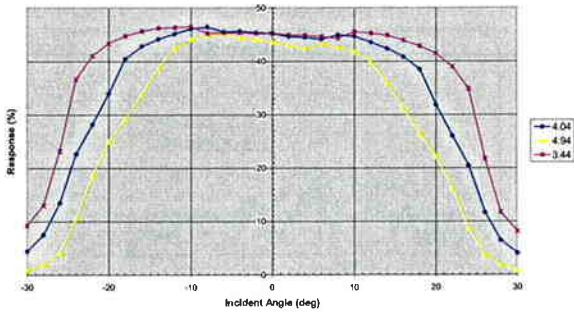


Fig. 7: Simulated angle response for 2.7 μm pixel. The Al layer has the most rapid reduction vs. angle; the reduced Cu has the least rapid.

	BEOL Stack thickness (4 LM, 3 LM over pixel)	Total thickness (incl. color filters) to base of lens	Simulated angle response for 2.7 μm pixel
Al	3.6 μm	4.9 μm	17
Cu	2.7 μm	4.0 μm	21
Reduced Cu	2.1 μm	3.5 μm	25

Fig. 8: Interconnect stack thickness and impact on angle response.

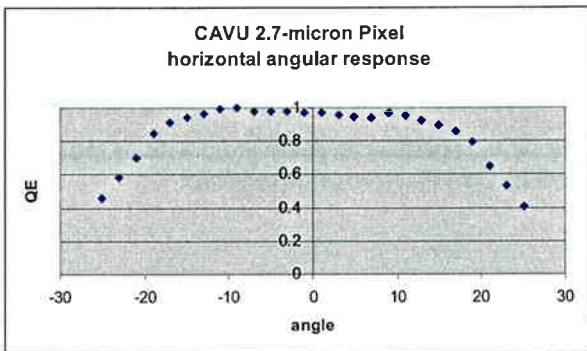


Fig. 9: Angle response for a 2.7 μm pixel. Compare to the intermediate model in Fig. 7.

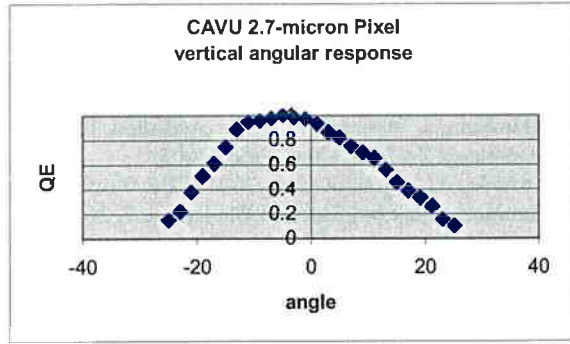


Fig. 10: Angle response in the short direction of the photodiode.

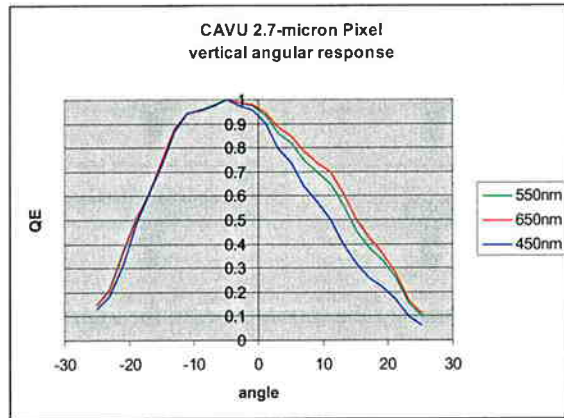


Fig. 11: Simulated angle response. Blue response is reduced due to absorption in the polysilicon gate.

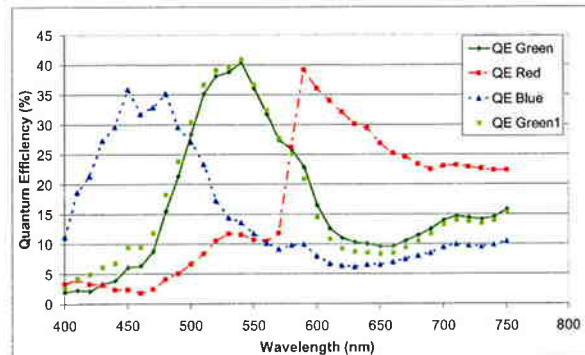


Fig. 12: Quantum efficiency of a 2.7 μm pixel with microlenses for red, green, and blue filters.