A High S/N Ratio CMOS Image Sensor with Real Time Object Categorizing Function

Shigetoshi Sugawa, Tomoyasu Tate, Koji Chiba, Koji Kotani and Tadahiro Ohmi[1]
Graduate School of Engineering, Tohoku University,
Aza-Aoba 10, Aramaki, Aoba-ku Sendai 980-8579, Japan Tel: +81-22-217-3977, Fax: +81-22-263-9395,
E-mail:sugawa@fff.niche.tohoku.ac.jp
[1]New Industry Creation Hatchery Center, Tohoku University

1. Introduction

A realization of image compression technology having high compression capability without degradation of image quality is demanded in order to improve with communication and storage efficiency of large volume image data. It is expected that image compression efficiency becomes high if image data are categorized by every object which resembled closely such as a person, natural scenery, article and character. High quality and high functionality CMOS image sensors have been developed [1-6], but an image sensor that has an object categorizing capability to achieve a high image-compression ratio has not been reported. In this paper, a fundamental technology of a high S/N ratio CMOS image sensor that has an object categorizing function for video-rate images is reported.

2. Image Sensor Device and Circuits

The unit of the CMOS image sensor photo-pixel peripheral circuit is shown in Fig.1. This unit is composed of a photodiode with complete charge transfer capability, a signal readout circuit with noise reduction and sample-hold function, a comparator, and a two times gain amplifier. The noise reduction operation for threshold voltage variations of MOS transistors and thermal reset noise at pixel floating diffusion node are achieved by a combination with a charge transfer operation from the photodiode to the floating diffusion and a sample-hold operation. The operation frequency of the sensor and amplifier are about 1MHz in order to minimize the flicker noise due to the interface trap state density between the silicon and gate insulator film of MOSFET. The 6-bits pipeline A/D conversion operations are carried out for each about 1ms period by serially connecting six sample-hold, comparator and amplifiers which are shared by some pixels shown in Fig.2. The digital signals after A/D conversion are stored in the resistors setting at the side of pixel area and are used in next ALU circuits for categorizing every object which resembled closely. Fig.3 and Fig.4 show a total circuit block diagram and a pixel array operation time chart of the sensor, respectively. The size of the photo-pixel unit is 30μmx30μm and the fill factor is 25% in designing with 0.35mm technology. Fig.5 shows the plane view of the pixels and peripheral circuits. Fig.6 (a) shows before the noise reduction characteristics of A/D conversion signal, Fig.6 (b) shows after and the number of remaining noise charge is reduced to about 5 electrons as an input conversion noise.

A higher packing density circuits than above pipeline A/D converter circuits are achieved by a time-axis sampling A/D conversion shown in Fig.7 and Fig.8. In this case, A/D converters are setting each pixels, and is operated by time-axis comparing operations in each sub-frame (~1ms) according to the time chart shown as Fig.9.

3. Real Time Object Categorizing Algorism

The object extraction algorithm is shown in Fig.10. The color difference is calculated as 4-bits Hue value angle. The simplified transform equation of CIE1960 uniform chromaticity scale system is described as follows;

$$H = Tan^{-1}\frac{G-B}{R-G}$$

where H is color difference.

It is difficult to implement this equation to the hardware circuit, so the solution of Tan^{-1} is simplified and calculated in this sensor shown as right hand side of Fig.10.

The texture is represented as a 4-bits difference value between maximum and minimum data in a reference and its neighboring eight pixels. In the 3x3 pixel block around a reference pixel, the luminance variation is converted to the space frequency.

The motion is calculated as a 1-bits deference value between sub-frame signal and another sub-frame signal. When the signal voltage variation is lager than a threshold voltage, the object sensing by the pixel are regarded as the motion object.

Finally, the range information is extracted from a deference value between two focused sub-frame signals obtained by lens focus motion. The lens motion is carried by manual operation in this experiment, but will be automatically operated in near future.

Fig.11 shows the circuit of ALU calculating the color difference, texture, motion and range information.

Fig.12 shows the examples of extract results of the color difference, texture, motion and range data and the final object categorizing result of 4-bits data.

The object categorizing operation are performed every video frame by sampling image data every about 1ms sub-frame. The 10-bits video signal and the 4-bits category number for each pixel are outputted from the sensor every 60 frame/sec.

4.Conclusion

A fundamental performance of a high S/N ratio CMOS image sensor with real time object categorizing function is demonstrated. The image sensor will be utilized in a communication and storage application field of high quality and large volume image data.

Reference

[1] S. K. Mendis, et al., IEEE Journal of Solid-State Circuits, 32(1997)187-197

[2] H. Takahashi, et al., IEEE Workshop on CCD & AIS, (2001)203-206

[3] S. Inoue, et al., IEEE Workshop on CCD & AIS, (2001)16-19

[4] I. Ishii, et al., Proc. IEEE Int. Conf Robotics and Automation, (1996)2309-2314

[5] S. Kawahito, et al., IEEE Journal of Solid-State Circuits, 32(1997)2030-2041

[6] K. Aizawa, et al., IEEE Workshop on CCD & AIS, (1999)R31

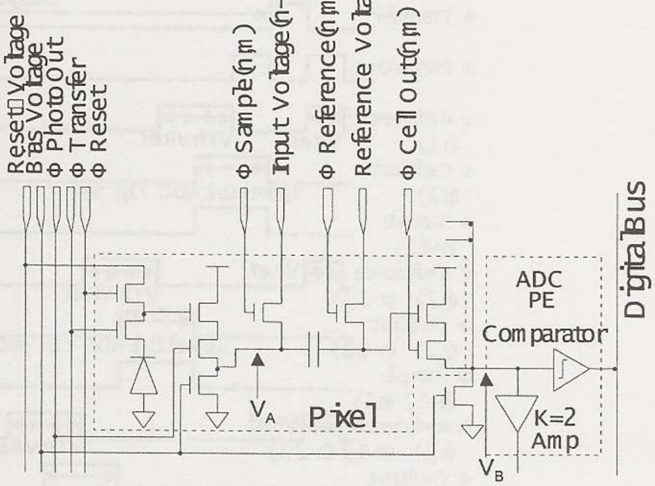


Fig.1 The unit of the CMOS image sensor photo-pixel peripheral circuit diagram

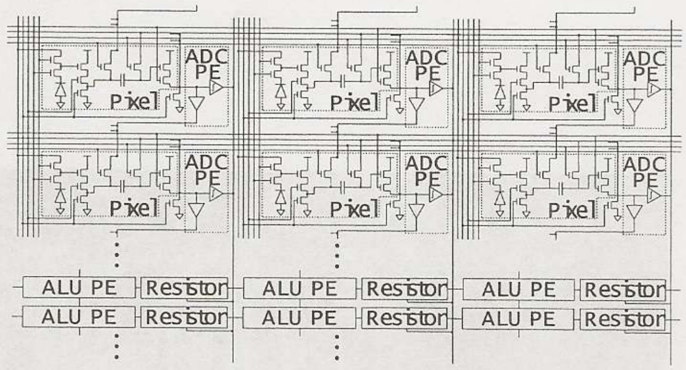


Fig.2 The serially connecting sample-hold, comparator and amplifiers circuit diagram

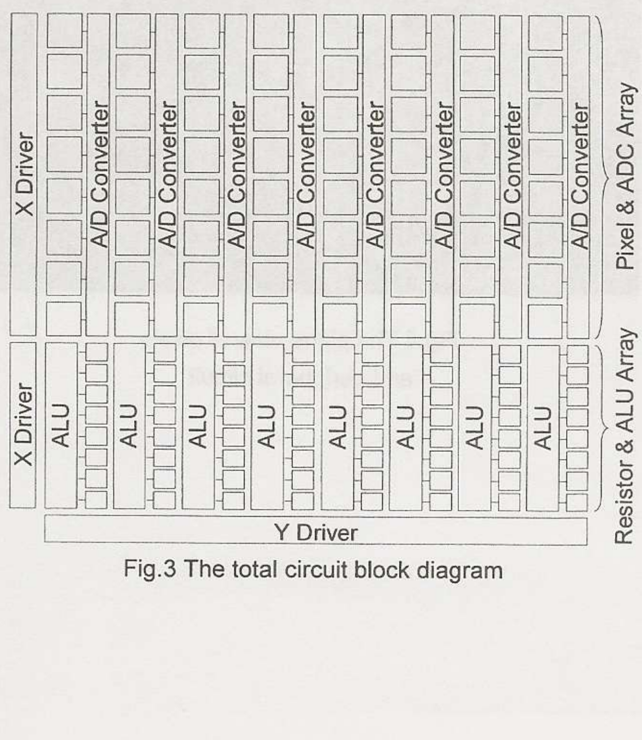


Fig.3 The total circuit block diagram

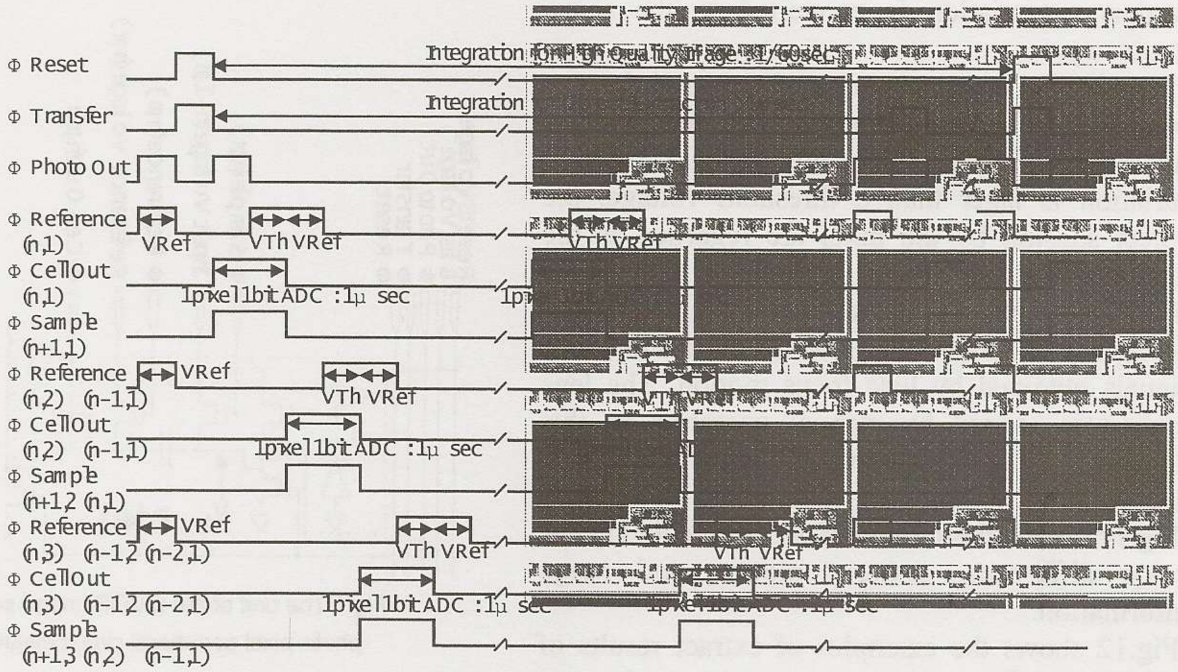


Fig.4 Time chart of pixel array

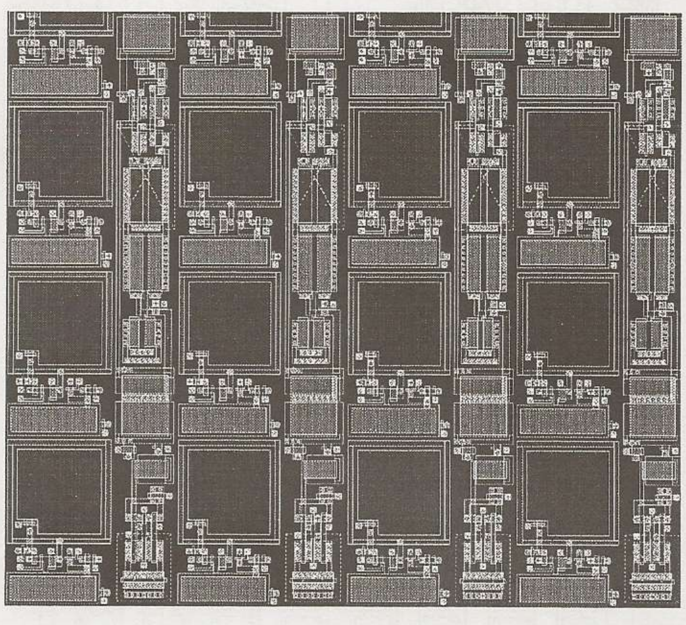
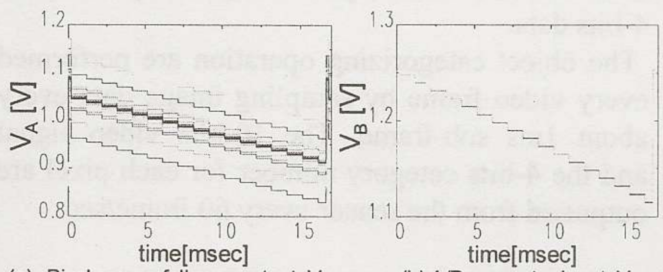


Fig.5 The plane view of pixels
and peripheral circuit



(a). Pixel source follower output, V_A (b) A/D converter input , V_B

Fig.6 The noise reduction characteristics

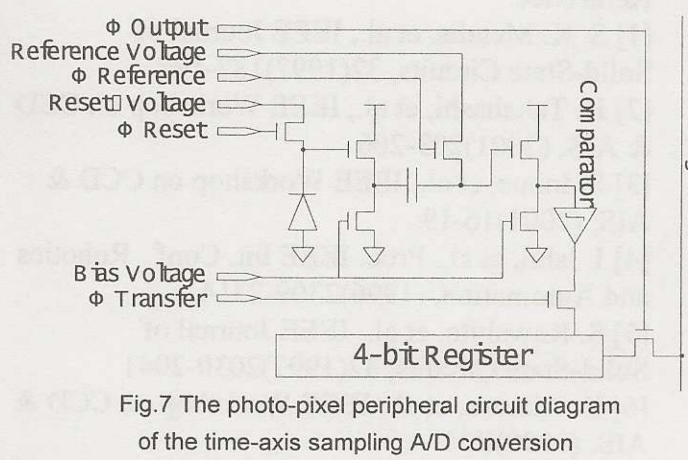


Fig.7 The photo-pixel peripheral circuit diagram
of the time-axis sampling A/D conversion

Φ Res
Φ Refe
Φ Tra

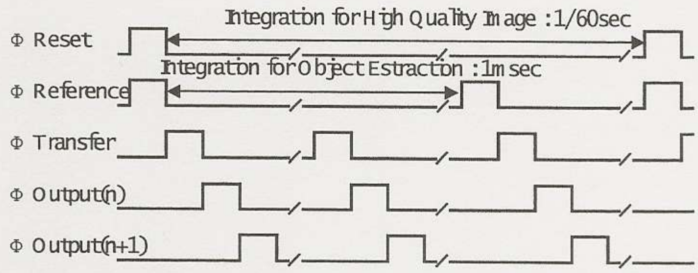
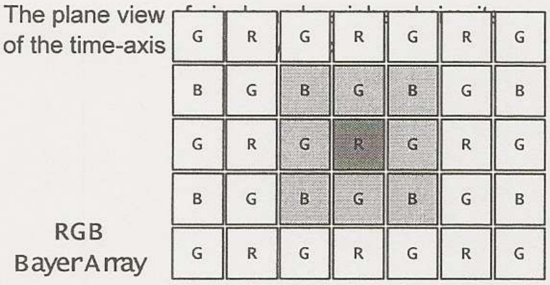


Fig.9 Time chart of the time-axis sampling A/D conversion

Fig.8 The plane view of the time-axis



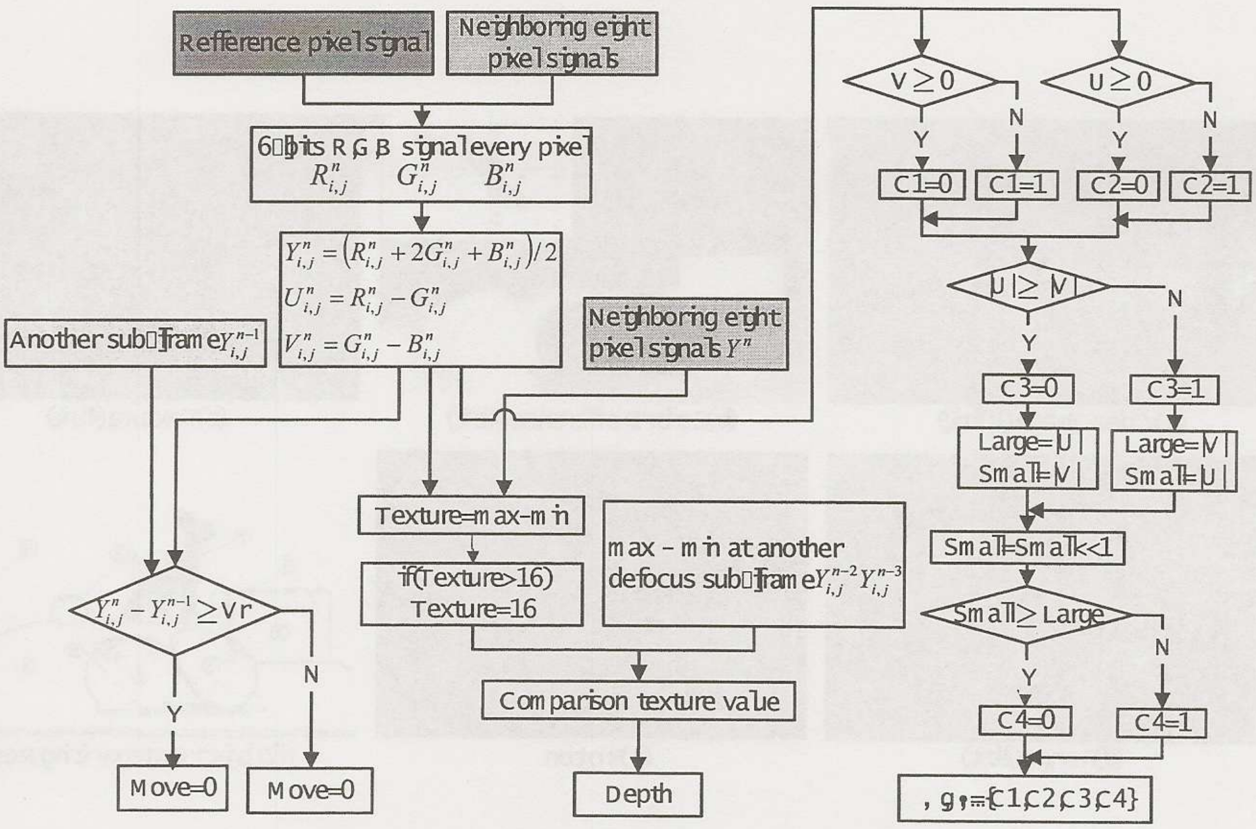
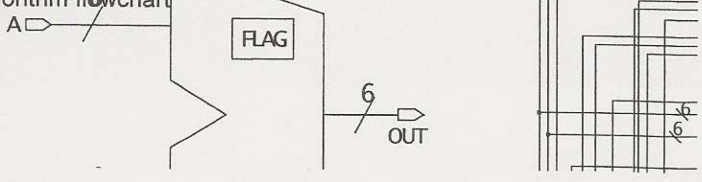


Fig.10 The object extraction algorithm flowchart



CB	OPERATION
0	ADD
1	XOR
2	LRS
3	LLS
4	COMP
5	SELECT
6	FLAG OUT
7	FLAG SET

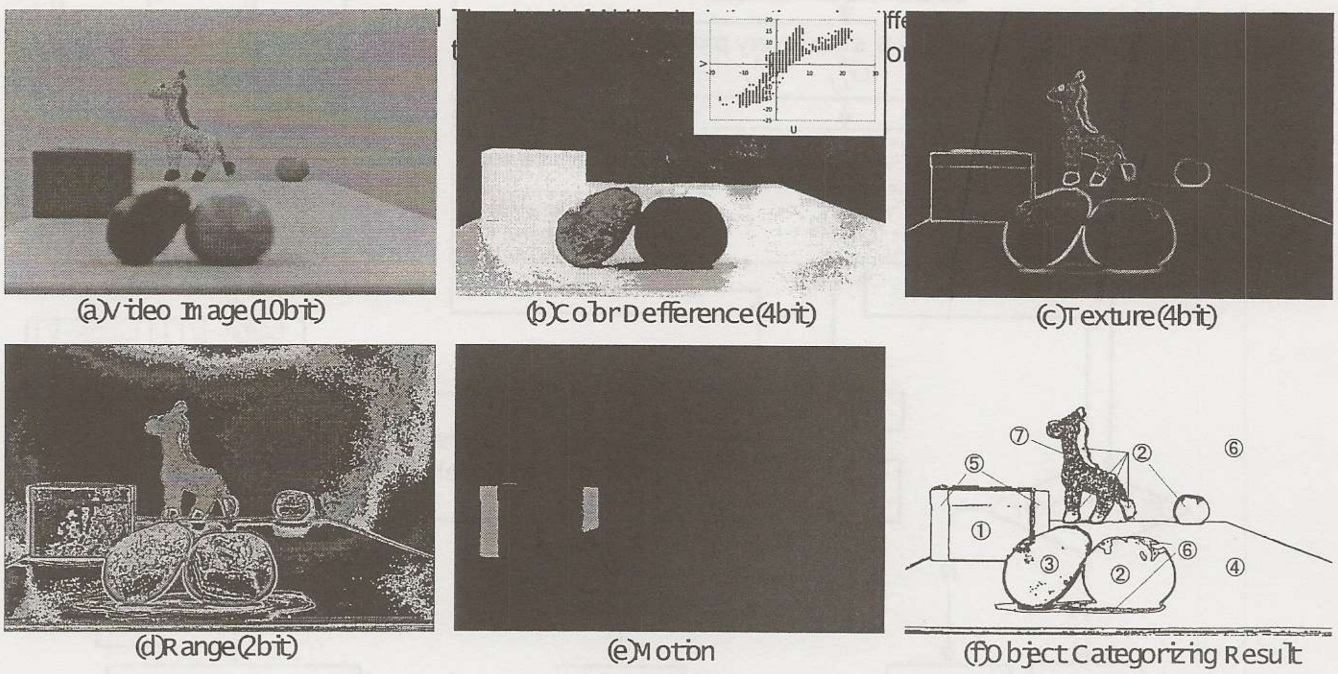


Fig.12 Result of the object extraction