

Backside-hybrid photodetector and image sensor for trans-chip detection of NIR light

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abstract Trans-chip NIR detection by a backside-hybrid photodetector is proposed. Numerical device simulation and experimental demonstration with a discrete N-Si/P-Si/N-Ge device are carried out. Photocurrent generated by NIR beam ($1.31\mu\text{m}$) was detected. In order to verify the feasibility, a CMOS photodetector array chip was designed.

1. Introduction

Si is transparent for NIR light with $\lambda > 1.2\mu\text{m}$ and no photocarrier is generated in that wavelength region. The NIR ($\lambda > 1.2\mu\text{m}$) imaging has been one of the expected breakthroughs. In order to extend the wavelength region without disturbing the function of Si image sensors, the authors propose trans-chip detection method using a NIR detection layer on the backside of an image sensor chip. The NIR detection layer enables the photogeneration by NIR ($\lambda > 1.2\mu\text{m}$).

2. Concept of trans-chip NIR detection

It is generally accepted that only the photocarriers generated in depletion regions contribute to the photocurrent. However, in some cases, diffusion of the photocarriers generated in field-free un-depleted regions is not negligible. Because carrier diffusion lengths can be larger than $100\mu\text{m}$ for Si substrates commonly used for CMOS processes, it may be possible to detect the photocarriers generated at the NIR detection layer. Although a lot of issues such as low sensitivity or severe smear should be overcome, this detection method is still promising because it does not require any modification on the image sensor architecture on the top surface.

Figs. 1-3 show a model structure and results of a computer-simulation of a trans-chip NIR photodetector. The photodetector was consisted of a N-diffused region ($1 \times 10^{16}\text{cm}^{-3}$)/P-substrate ($1 \times 10^{14}\text{cm}^{-3}$) photodiode (PD) and a Ge NIR detection layer on the backside, as shown in Fig. 1. The Ge layer was assumed to be N-type ($1 \times 10^{17}\text{cm}^{-3}$) in this model. Simulations for different Ge thickness were carried out. Fig. 2 shows a band diagram of the device under a reverse bias of 10V. The thickness of the Ge NIR detection layer was $5\mu\text{m}$. Fig. 2 shows that the Ge NIR layer on the backside is not under depleted situation. Fig. 3 shows the simulated responsivity at $\lambda = 1.3\mu\text{m}$ for the thickness of the Ge layer of 1, 5, $10\mu\text{m}$. Although the backside P-Si(substrate)/N-Ge junction is under nearly non-biased condition(Fig. 2), a photocurrent is observed, as shown in Fig. 3. This simulation suggests that the backside N-Ge layer enables the trans-chip NIR detection. It is clearly shown that the responsivity depends on the thickness of the Ge layer.

3. Experimentals

A discrete photodetector was fabricated to demonstrate the trans-chip NIR detection. Fig. 4 shows the structure of the photodetector. A $50\mu\text{m}$ -thick P-Si ($4\text{-}10\ \Omega\text{cm}$) substrate was used. A N-diffused layer was formed by diffusion from a phosphorus-doped spun-on SiO_2 layer. Referring provided process data, the X_j and the sheet resistance are estimated to be $2\text{-}5\mu\text{m}$, and $10\text{-}20\ \Omega/\text{cm}^2$, respectively. A mesa structure was formed by a wet etching process. A $1\mu\text{m}$ -thick Ge layer was deposited onto the backside of the wafer by solid-source molecular beam epitaxy (MBE). The substrate temperature was 300°C ., and the growth rate was 60nm/h . The Ge layer shows N-type

conduction ($>1 \times 10^{18} \text{cm}^{-3}$) in Hall measurements, and it is highly defective because of a high density of misfit dislocations and the low growth temperature. Fig. 5 shows I-V characteristics of the photodetectors. As shown in Fig. 5, the deposition process of the Ge layer deteriorates the I-V characteristic of the Si PD and it should be overcome by optimizing the growth conditions. In order to cancel the dark-current, a photocurrent was measured under a modulated illumination. A $1.31 \mu\text{m}$ LD beam modulated with 10Hz was illuminated onto the photodetector from the top surface. The power of the beam was 8.2mW. The photocurrent was in the order of $10^{-8} - 10^{-7} \text{A}$, which corresponds to a responsivity of $0.3 - 2 \mu\text{A/W}$. Fig. 6 shows the responsivity as a function of the bias voltage. A bias-dependent increase was observed similarly to the simulation (Fig. 3). However, the responsivity of the photodetector is smaller than that expected from the simulation (Fig. 3). The authors suspect that the poor crystalline quality of the Ge layer causes this smaller responsivity. This small responsivity is the essential issue for the trans-chip detection.

4. Design of a trans-chip NIR detector array

The most advantageous point of the trans-chip NIR detection is the compatibility with conventional image sensor architectures. Fig. 7 schematically shows a concept of the trans-chip NIR detection implemented onto a CMOS image sensor. The function of NIR detection can be controlled by bias conditions, and it can be completely deactivated if necessary. A photodetector array chip was designed to verify the feasibility of the trans-chip detection concept. Fig. 8 shows an appearance of the chip layout. The fabrication process is $0.6 \mu\text{m}$ CMOS 2 poly 3 metal. In order to drive the photodetector array applying a negative bias voltage on the substrate, all the circuits were implemented with PMOS devices, which are isolated from the substrate by N-wells. In order to improve the isolation between PDs and reduce a smear, a N-Well or N-diff ring surrounding the PD was adopted. The chip is under process optimization.

5. Summary

The trans-chip NIR detection by a backside-hybrid photodetector is proposed and demonstrated with a discrete N-Si/P-Si/N-Ge device. A photocurrent generated by NIR beam ($1.31 \mu\text{m}$) was detected. In order to verify the feasibility, a CMOS photodetector array chip was designed.

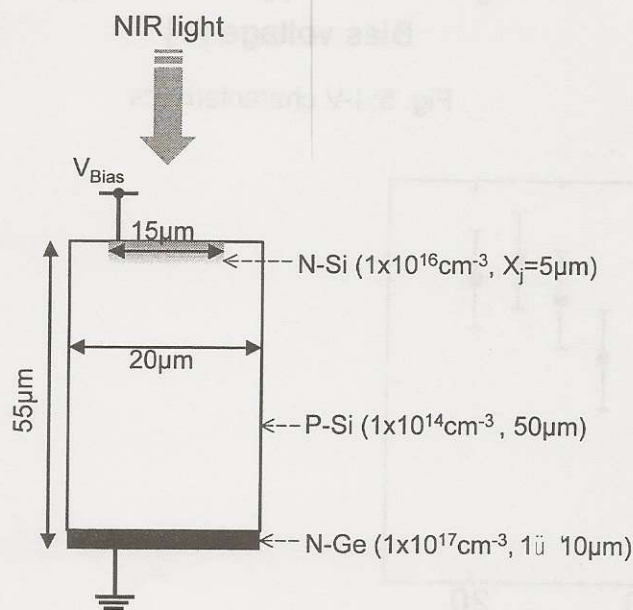


Fig. 1 Simulation model of a trans-chip NIR photodetector

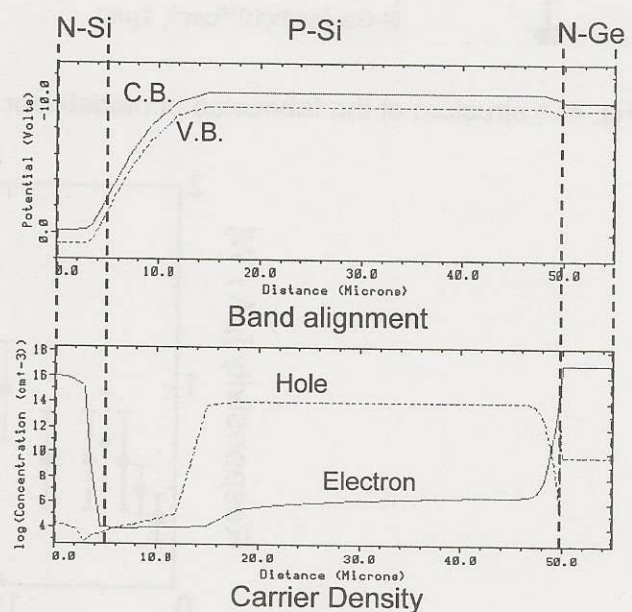


Fig. 2 Potential / Carrier profiles of the photodetector

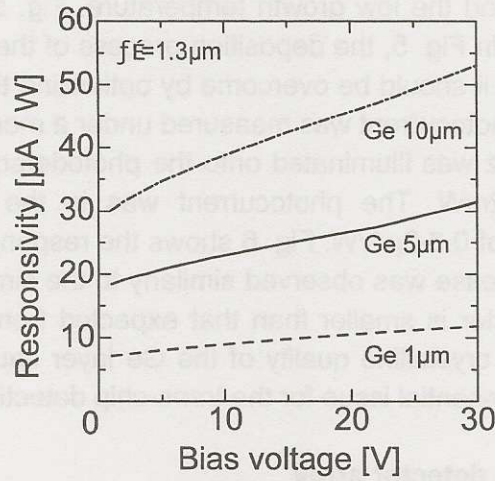


Fig. 3 Simulated responsivity (for 1.3μm) of the trans-chip NIR photodetector.

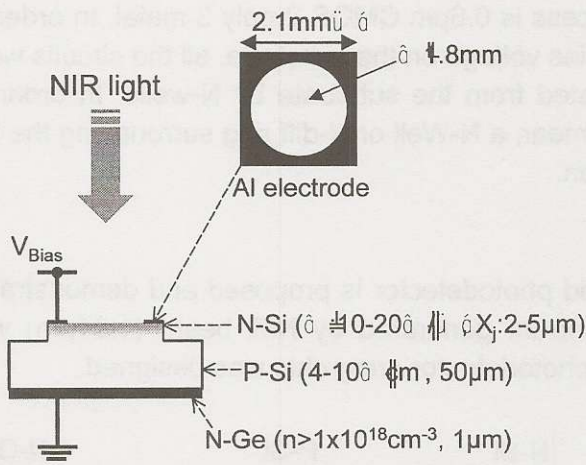


Fig. 4: A structure of the fabricated photodetector

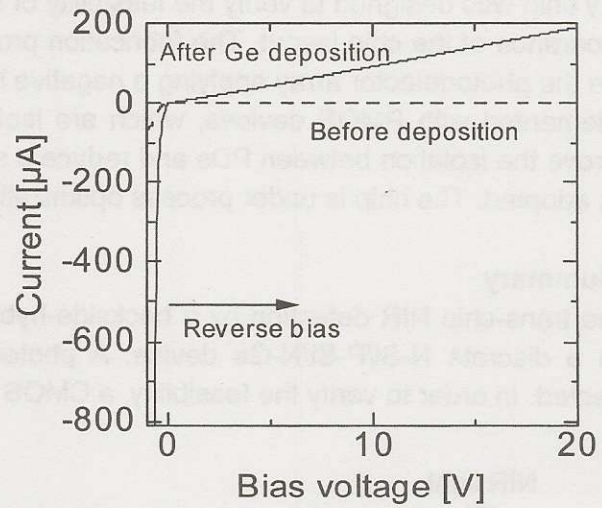


Fig. 5: I-V characteristics

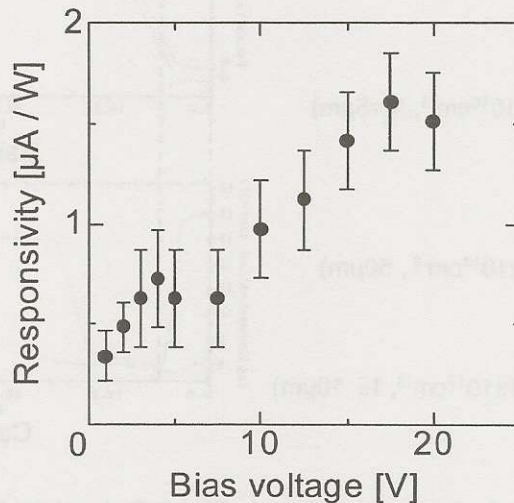


Fig.6: NIR (1.31μm) responsivity of the fabricated photodetector

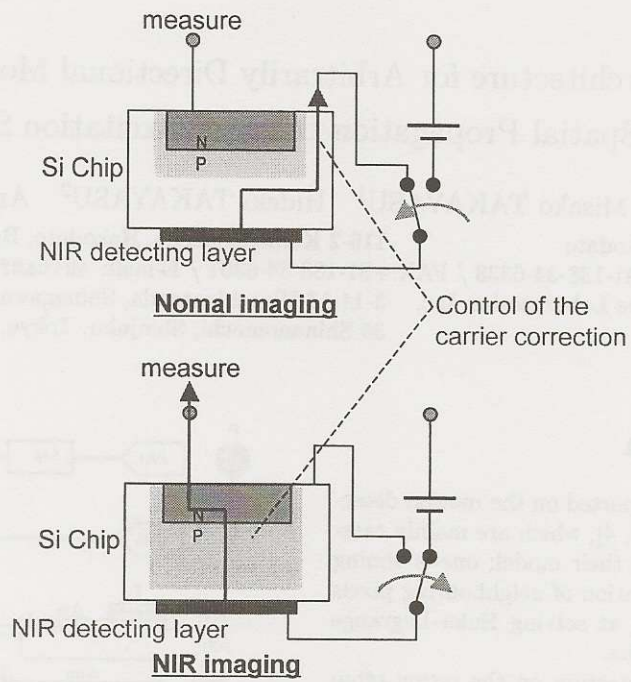


Fig. 7: A concept of the compatibility with CMOS image sensors

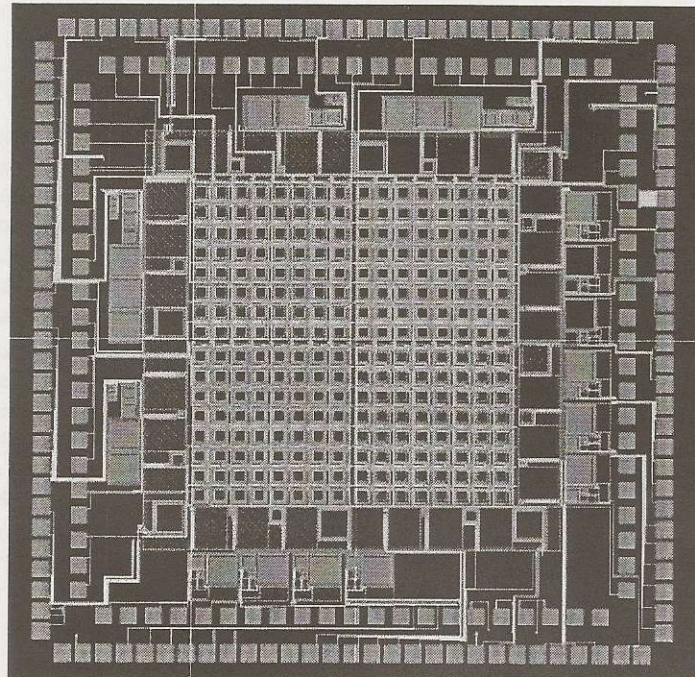


Fig. 8: Layout of the photodetector array for the trans-chip NIR detection