

CMOS IMAGE SENSOR WITH CUMULATIVE CROSS SECTION READOUT

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ABSTRACT:

Solid state image sensors are used in a large and growing array of applications. Moving beyond simple digital photography, the CMOS image sensor is capable of acting as a highly intelligent information collector by integrating image processing circuitry on the same chip as the sensor. This paper focuses on providing object location information with a smart CMOS image sensor. An architecture is presented for integrated high speed object location. This data can enable high speed detection of object location without the need to scan the entire frame, and can be further processed to find a high accuracy centroid. Possible applications for this technology include robotics, LIDAR, optical communications links, astronomy and industrial monitoring.

I. INTRODUCTION

A key driver of CMOS image sensor adoption is the ability to integrate signal processing circuits on the same chip as the imaging array. Extracting key information from an image is more important than the image itself in many applications. This paper presents a method of extracting object location information on-chip, providing savings in time and power consumption.

Previous work [1] took the form of a binary object location system, which included thresholding the integrated photo-voltages to create a binary image, and readout of this image through row and column wise ORing of the binary flags (Figure 1). A sample application for this extracted information is a multiple threshold algorithm to accurately calculate the centroid of an object in the image, which was demonstrated with a more accurate comparator and in-pixel pattern noise reduction circuit [2].

Other related work has been done in the past. The use of a CMOS image sensor as a receiver in a free-space optical communications system has been reported [3],[4], including the benefit of monitoring a large field of view. Several papers have discussed use of CMOS image sensors for star tracking to provide orientation data for satellite guidance [5],[6],[7]. Additionally,

work has been done with on-chip centroiding. Use of a resistive network to calculate a centroid has been proposed [8]. Calculating a centroid with an aggregation network of differential transistor pairs has been shown by [9]. The above approaches are relatively complex. A simpler technique was reported by [10]. Wide range in-pixel amplifiers were used as comparators, to generate a binary signal for each pixel, which were then summed at the edge of the array.

We report a similar approach here, however we also address issues of centroid accuracy and it's improvement by using multiple threshold values, pixel parallel operation, and system speed. This paper describes a novel cumulative cross section readout scheme. This scheme allows more information acquisition than our previous binary object location system, while maintaining the speed advantage of that approach. Instead of ORing the active pixels in a row or column, the CCS system will add them using current quanta supplied by in-pixel current mirrors (Figure 2).

II. ARCHITECTURE

The cumulative cross section pixel contains a photodiode and 12 transistors (Figure 3). A PMOS reset transistor is used to help reduce V_T non-uniformity between pixels. The photo-voltage is integrated over the frame period, and is compared to a reference threshold by a differential comparator, which is a standard design similar to those used for in-pixel ADCs [11]. An inverter is used to drive the comparator output rail-to-rail, producing in effect a binary flag which indicates whether or not the pixel's photo-voltage has dropped below the reference threshold voltage. When this occurs, it indicates that the incident illumination on the pixel exceeds the desired illumination threshold. Two current mirrors in the pixel are enabled when the threshold is exceeded, drawing a quantum of current through the output line. The chip was designed to use current quanta of around 10 μ A. Separate outputs are provided for the column and row directions, with one current mirror output to each.

At the end of each column and each row, each current quantum flows through a reference resistor, creating a

voltage drop from VDD which is proportional to the number of active pixels in the row or column (Figure 4). Thus current summation provides a sum of the number of pixels which exceed the threshold. In the prototype chip, this voltage is then read out of the chip with a row/column select signal and a unity gain amplifier to drive the output pad. However, in a commercial implementation the cumulative cross section voltages along the edges of the array could be the inputs to further information processing circuitry.

III. RESULTS

A prototype 80×80 pixel CMOS image sensor was fabricated in a standard CMOS $0.18 \mu\text{m}$ process (Figure 5), using $12 \times 12 \mu\text{m}$ pixels with a 51% fill factor (Figure 6). The prototype showed good linearity (Figure 9), and acceptable non-uniformity (Figure 10), considering a standard CMOS process was used. Unlike with a conventional APS sensor, these metrics had to be evaluated with respect to the switching characteristics of the pixels in aggregate. Measurements were carried out with a controlled digital light source and an optical integrating sphere to insure uniform illumination. Sensor operation becomes less linear at higher frame rates.

Testing confirmed proper operation of the prototype imager, using an LED as a light source in the field of view. Figure 11 shows prototype sensor output when an LED is presented in front of the sensor, approximately 30 cm distant. A lens was included in the setup. Two image frames are presented. In the second frame, the LED has been moved to the left, and kept in approximately the same position vertically. Reasonable detection of the LED was shown to be feasible at frame rates exceeding 1000 fps.

Table 1: Prototype chip summary

Physical Characteristics	
Die Size	3 x 2 mm
Technology	0.18 μm CMOS
Array Dimensions	80 x 80 (6400) pixels
Pixel Dimensions	12 x 12 μm
Transistors per Pixel	12
Fill Factor	51%
Performance	
Max Frame Rate	1600 fps
Dark Power	8mW
Saturated Power	~30mW

A more advanced prototype could incorporate dynamic tuning of the row data resistor R_{data} (Figure 4) to provide good discrimination for small objects while still

being able to work with large objects. This would be particularly useful when scaling to a high resolution imaging array.

IV. HIGH ACCURACY CENTROIDING

One application for our object location technology is on-chip centroiding. In order to refine the accuracy of a centroid calculation, multiple threshold values can be used. Multiple-threshold centroiding was originally conceived to operate with the basic binary object location system (Figure 1).

The additional data provided by the cumulative cross section readout scheme allows this centroiding algorithm to become even more effective. Very few threshold values are needed to determine a very accurate centroid. Results of MATLAB simulations of centroiding accuracy for a wide range of Gaussian light spots are shown in Figure 7. This algorithm was not implemented in hardware, but this would be a fairly easy addition to the design.

V. DIGITAL ARCHITECTURE

A brief overview of the next generation digital cumulative cross section readout will be touched on. The design was modified, with the current mode addition of binary flags replaced with digital accumulation. Digital adders were added to each pixel, along with in-pixel FPN suppression (Figure 8). The chip also includes an implementation of an algorithm making use of the digital CCS data to automatically determine a region-of-interest around the largest object. This region can then be read out, using standard APS pixel architecture, and the limited size of the region allows high speed readout of the region of interest.

VI. CONCLUSIONS

A prototype image sensor with a new cumulative cross section readout architecture is reported. Reducing image information to what is required for the application can allow higher readout rates for the sensor. The data provided by CCS readout can be used for a high accuracy centroid calculation. Integrating object location with the sensor holds the promise of lowering system power, cost and size.

VII. ACKNOWLEDGEMENTS

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VIII. REFERENCES

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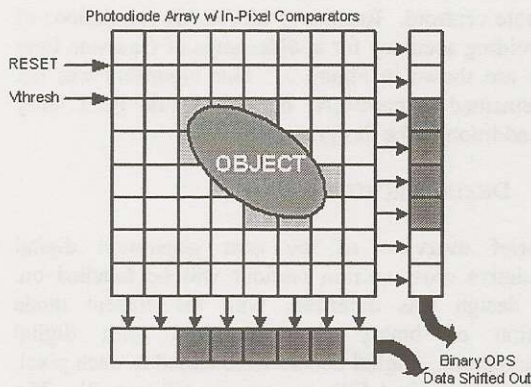


Figure 1: Operation of binary object location system. Image is binarized, and then data indicating which rows and columns contain active pixels is read out.

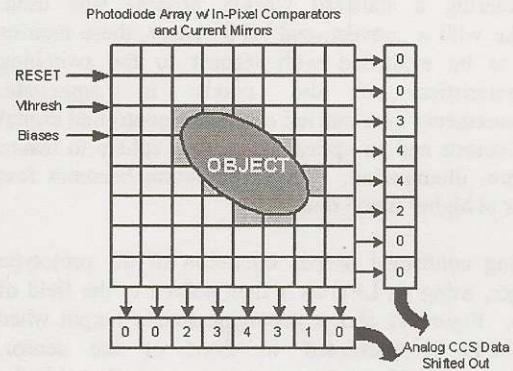


Figure 2: System operation of the Cumulative Cross Section (CCS) readout scheme. Image is binarized, and number of active pixels in each row and column is summed by current-mode addition.

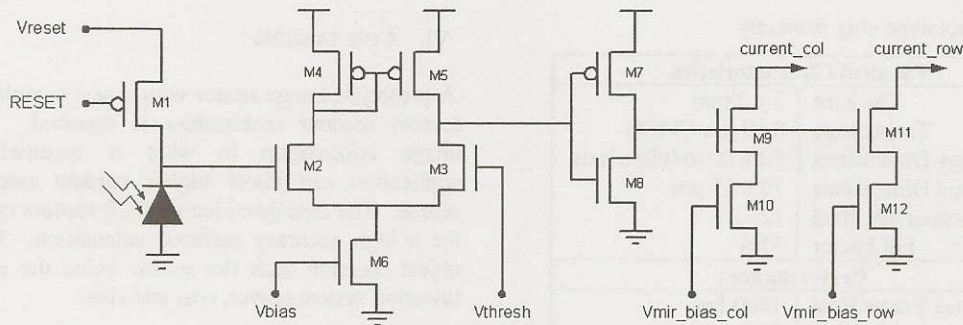


Figure 3: Schematic of pixel circuit for CCS chip. Each pixel contains a differential comparator and current mirrors for CCS readout.

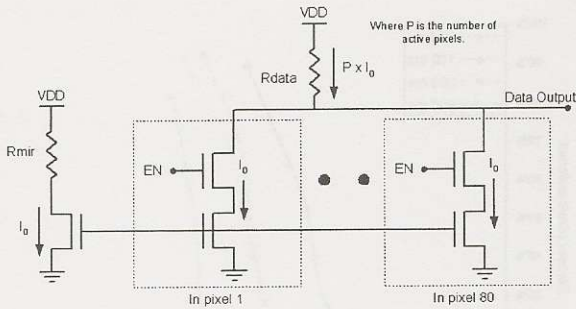


Figure 4: Output schematic for CCS readout. Each pixel contains a current mirror which draws a quantum of current when active. These currents cause a voltage drop across R_{data} , which is proportional to the number of active pixels.

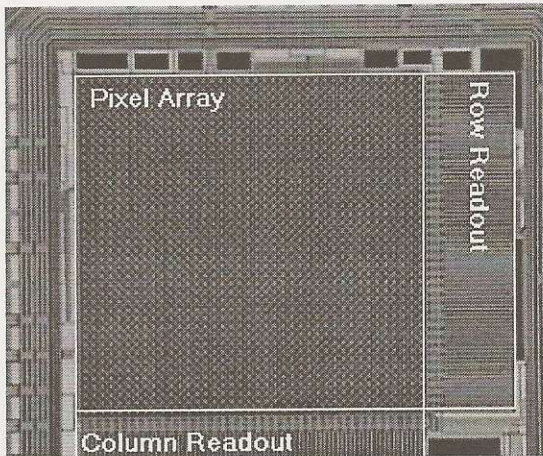


Figure 5: Photomicrograph of prototype CCS chip.

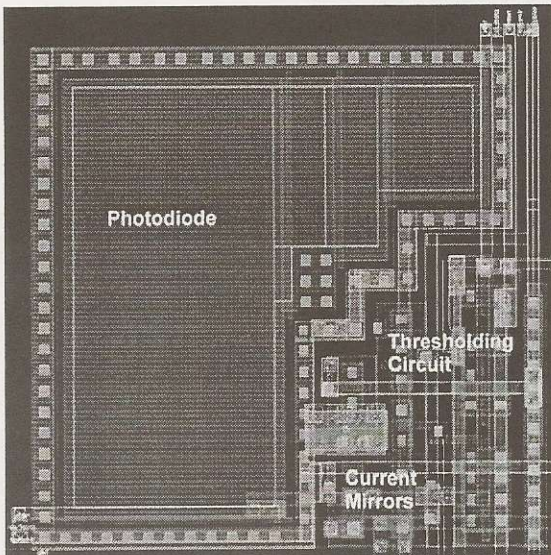


Figure 6: Layout of cumulative cross section pixel.

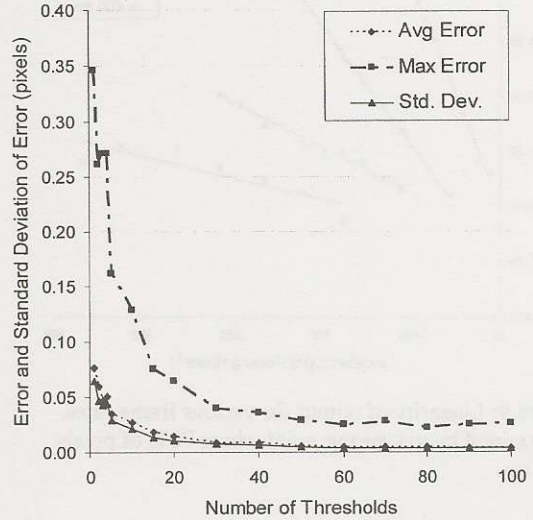


Figure 7: Simulated multi-threshold centroid accuracy for a range of varied Gaussian bright spots.

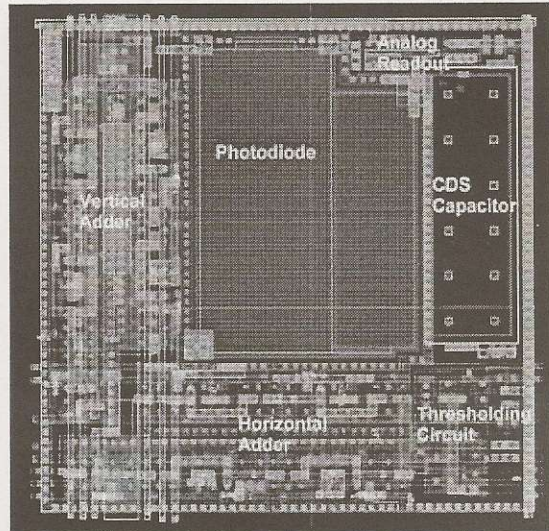


Figure 8: Layout of next generation digital cumulative cross section pixel.

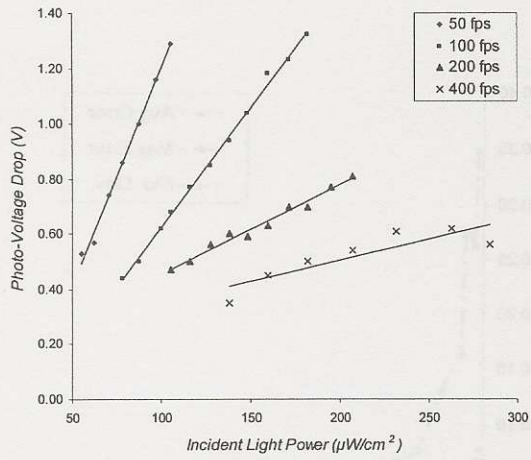


Figure 9: Linearity of output for various frame rates. Determined by measuring point where 90% of pixels were on.

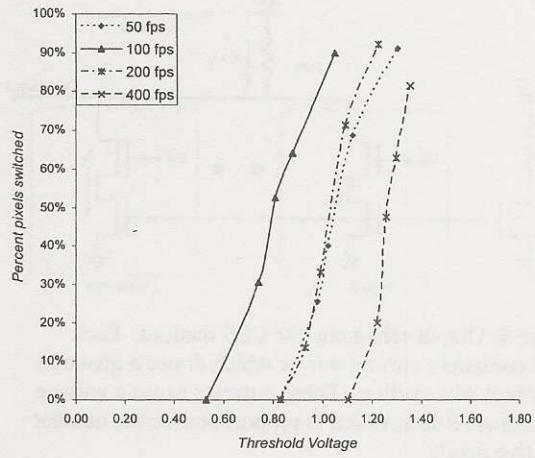


Figure 10: Switching non-uniformity of prototype CCS imaging chip. Different light intensities were used at each frame rate to provide sufficient illumination.

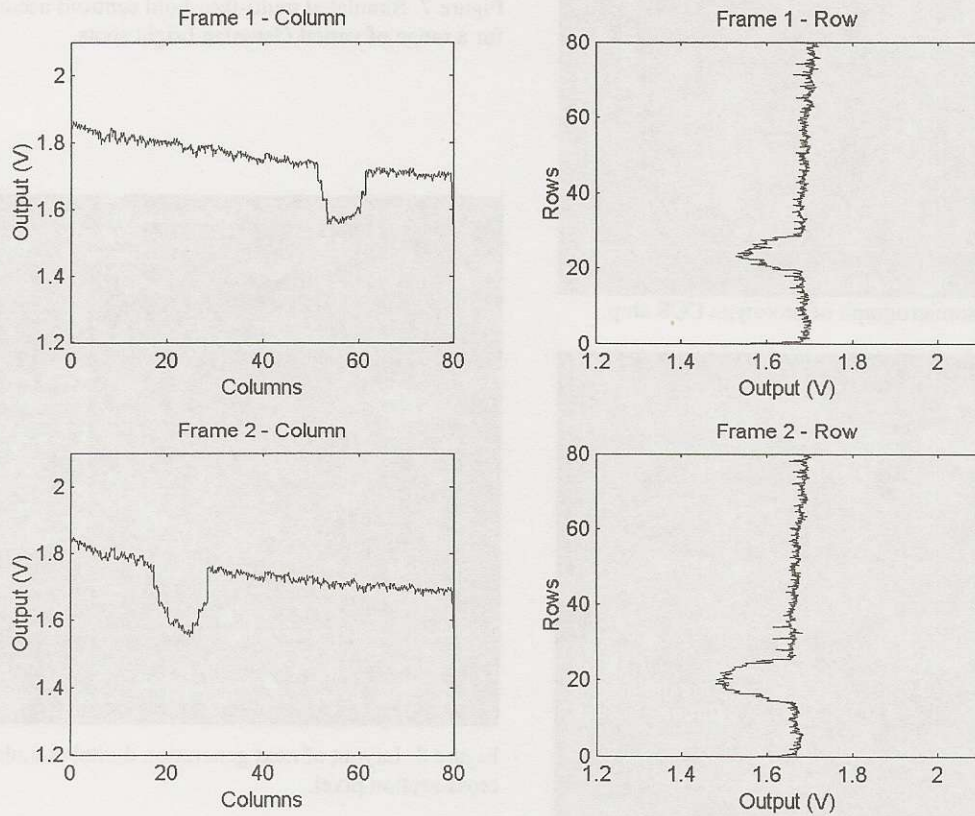


Figure 11: Corrected output showing LED in the lower part of the imager, moving right to left in the sensor's field of view. Image captured with prototype chip at 100 frames/s.