3-D Optical and Electrical Simulation for CMOS Image Sensors

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Abstract

The readout and crosstalk characteristics of CMOS image sensors are analyzed by a 3-D device simulator SPECTRA and a 3-D optical simulator TOCCATA. It is found that the time constant of readout operation strongly depends on readout gate shape and the main source of crosstalk is diffusion current induced by long wavelength light. The light gathering power of micro-lens dependence on cell size analyzed by 3-D wave optical simulation extremely decreases with reduction of cell size in the region less than 2 μm and strongly depends on the shape of photo-sensitive region.

I. Introduction

Since the most of the applications of CMOS image sensors need small chip size and high resolution simultaneously, the pixel size has been reduced with the progress of lithographic technology. The reduction of pixel size makes it difficult to design cell structures ignoring 3-D effect such as narrow channel effect of photodiode potential, because the buried photodiode with deep depletion region is necessary to realize low dark current and small image lag [1]-[4]. To analyze the optical and electrical characteristics of CCD image sensors, a 3-D device simulator SPECTRA and a 3-D optical simulator TOCCATA have been developed [6]. The combination of the above simulators seems to be powerful even for the analysis of CMOS image sensors, because most of the models for CCD image sensors should be adopted to the analysis for CMOS image sensors without modification. In this paper, simulation results for readout and crosstalk characteristics of CMOS image sensors and the light gathering power of micro-lens dependence on cell size are reported.

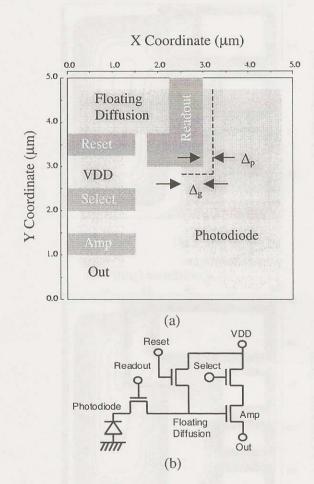
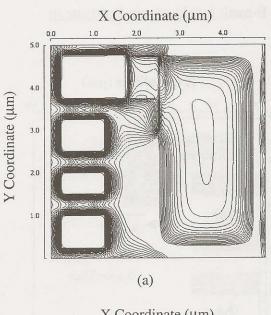


Fig. 1. Cell structure for readout analysis. (a) Gate and diffusion layout. (b) Equivalent circuit. Δ_g denotes the distance between the readout gate right side edge and the photodiode left side edge. Δ_p denotes the distance between the readout gate edge and the photodiode P+ doping mask edge.

II. Readout

Fig. 1 (a) shows the cell layout for the readout operation analysis. The 5 x 5 μ m² cell consists of a buried photodiode and four MOS transistors (for readout, reset, select, and amplification functions),

fabricated in p-type substrate [1]-[5]. The equivalent circuit is shown in Fig. 1 (b). The power supply voltage is assumed to be 3.3 V. Δg denotes the distance between the readout gate right side edge and the photodiode left side edge. Δp denotes the distance between the readout gate edge and the photodiode P+ doping edge. The readout characteristics dependence on Δg , Δp , and photodiode relative donor concentration Npd was calculated.



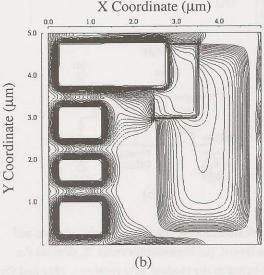


Fig. 2. Maximum potential in the XY-plane during readout operation. (a) Δ_g = 0, Δ_p = 0.25. (b) Δ_g = 1.0, Δ_p = 0.1.

Fig. 2 shows the 2-D maximum potential in the XY-plane during readout operation in the case of $\Delta_{\rm g}$ = 0, $\Delta_{\rm p}$ = 0.25 and $\Delta_{\rm g}$ = 1.0, $\Delta_{\rm p}$ = 0.1. Fig. 3 shows the 1-D maximum potential along X-axis, where $\phi_{\rm pd}$,

 $\phi_{\rm b}, \ \phi_{\rm dip}, \ \phi_{\rm g}$, and $\psi_{\rm fd}$ denote potential of photodiode, barrier, dip, gate, and quasi-Fermi potential of floating diffusion, respectively. The barrier height $\phi_{\rm pd}$ - $\phi_{\rm b}$ and the potential dip $\phi_{\rm dip}$ - $\phi_{\rm g}$ dependence on Δg and Δp are shown in Fig. 4.

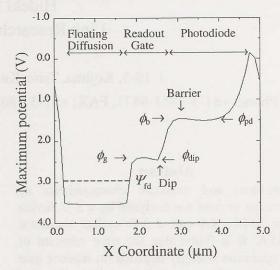


Fig. 3. Maximum potential along X-axis during the readout operation in the case of Δ_g =0 and Δ_p =0.25. ϕ_{pd} , ϕ_b , ϕ_{dip} , ϕ_g , and ψ_{fd} denote potential of photodiode, barrier, dip, gate, and quasi-Fermi potential of floating diffusion, respectively .

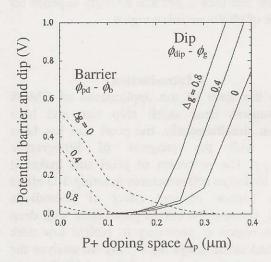


Fig. 4. The barrier height $\phi_{\rm pd}$ - $\phi_{\rm b}$ and the potential dip $\phi_{\rm dip}$ - $\phi_{\rm g}$ dependence on $\Delta_{\rm g}$ and $\Delta_{\rm p}$. Solid line: potential dip. Broken line: barrier height.

Although ϕ_{pd} - $\phi_b = 0$ and ϕ_{dip} - $\phi_g = 0$ cannot be satisfied simultaneously for any Δ_p in the case of $\Delta_g = 0$, some margin of Δ_p exists in the case of Δ_g more than 0.4 μ m. Even if there is small potential barrier or small potential dip around the readout gate edge, it is possible for the signal charge to spill over the barrier or the dip, because of thermal diffusion. In such a case, since the amount of remained charge in

photodiode strongly depends on readout time, transient simulation is necessary. The remained photodiode charge dependence on time in the readout operation is shown in Fig. 5, where thermal diffusion is considered. The photodiode charge can flow over small potential barrier or dip by thermal diffusion. It is found that the readout time can be reduced from 100 ns to 10 ns by increasing Δg from 0 to 1.0 μm .

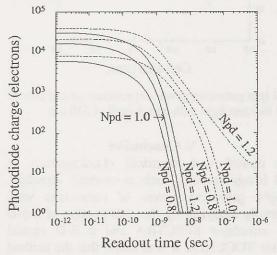


Fig. 5. Remained photodiode charge dependence on readout time. Solid line: Δ_g =1.0. Broken line: Δ_g =0. N_{pd} is photodiode relative donor concentration.

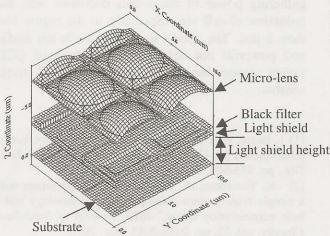


Fig. 6. Structure with micro-lens for ray-tracing simulation, which consists of four pixels.

III. Crosstalk

Fig. 6 shows the micro-lens structure for optical crosstalk analysis. The distribution of incident light angle is assumed to correspond to F-number of 2.0. The optical crosstalk dependence on the light shield height is shown in Fig. 7, where vertical, horizontal, and diagonal, denote the light power ratio at left top, right bottom, and right top photo-sentive area against the light power at the left bottom

photo-senstive area. Fig. 8 shows the electronic crosstalk dependence on wavelength. The fact that the longer wavelength induces the larger electronic crosstalk indicates that the main source of the electronic crosstalk is the diffusion current induced by long wavelength light. The electronic crosstalk of P-well in n-type substrate structure [2], [4] is much smaller than that of P-type substrate structure, because P-well in n-type substrate structure prevents the diffusion current from deep substrate region to photodiode.

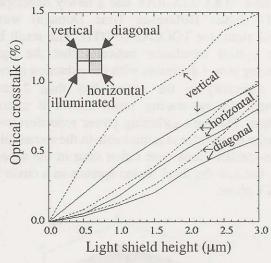


Fig. 7. Optical crosstalk dependence on light shield height. Solid line: with micro-lens. Broken line: without micro-lens.

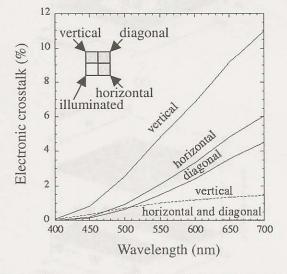


Fig. 8. Electronic crosstalk dependence on wavelength. Solid line: p-type substrate. Broken line: P-well in n-type substrate.

IV. Light gathering power of micro-lens

Fig. 7 shows the structure for the analysis of micro-lens light gathering power dependence on cell size in the case of 25 % aperture ratio. The every length, the radius of sphere micro-lens, the distance between micro-lens and silicon substrate, and aperture size of photo-sensitive region, is proportionally changed with cell size. The light gathering power dependence on cell size by vertical incident light with wavelength of 550 nm is shown in Fig. 8, which is calculated by a ray-tracing simulator TOCCATA-RAY and a newly developed FDTD (Finite Difference Time Domain) wave optical simulator TOCCATA-FDTD. The result by wave optical simulation indicates that the light gathering power decreases with the reduction of cell size especially in the region less than 2 µm, although the ray-tracing result shows it almost constant. The light gathering power reduction with decrease of cell size is remarkable in the rectangular photo-sensitive area case rather than in the square case, because the focal region spreads as a circle in the XY-plane.

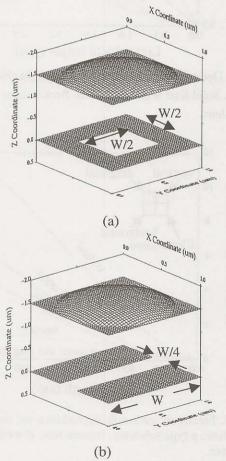


Fig. 7. Structure for wave optical simulation of light gathering power dependence on cell size. (a) Square photo-sensitive region. (b) Rectangular photo-sensitive region.

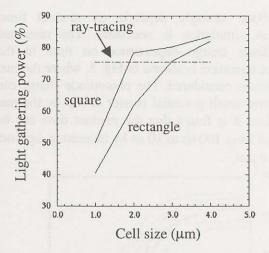


Fig. 8. Light gathering power dependence on cell size by vertical incident light with wavelength of 550 nm.

V. Conclusion

The optical and electrical characteristics of CMOS image sensors, such as readout, crosstalk, and light gathering power of micro-lens were successfully analyzed by the combination of a 3-D device simulator SPECTRA and a 3-D optical simulator TOCCATA. It was found that the readout time can be reduced by changing the readout gate shape, the crosstalk can be improved by using P-well in n-type substrate structure, and the light gathering power of micro-lens decreases with the reduction of cell size especially in the region less than 2 μm . The above simulation tools are useful and powerful not only for the analysis of CCD image sensors but also for that of CMOS image sensors.

References

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