A CMOS Image Sensor with Gain-Adaptive Column Amplifiers

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1. INTRODUCTION

CMOS image sensors have advantages of low-power consumption, single supply voltage, and capability of on-chip system integration in contrast with CCD image sensors. However, their image quality in low light level is not yet compatible with the CCD. This paper presents a CMOS image sensor with gain-adaptive column amplifiers and a pinned photodiode technology. The use of high gain at the column of CMOS image sensors is effective for reducing the random read noise. However, for a large pixel output signal, the high-gain column amplifier will saturate. To avoid this problem, pixel gain is adaptively changed using a comparator array at the column. The use of high gain at the column also leads to a high precision FPN canceling in digital domain.

The implemented CMOS image sensor shows low noise characteristics and the resulting dynamic range is comparable to the standard CCD image sensor.

2. PRINCIPLE AND OPERATION

Figure 1 shows the block diagram of the CMOS image sensor developed. The major random noise sources in low light level are the reset noise, the dark current shot noise, and the read amplifier noise. Among these, the reset noise and the dark current shot noise are suppressed by a pinned photo diode technology [1][2][3]. To suppress the read amplifier noise and the fixed pattern noise, this image sensor has low-noise high-gain column amplifiers. To avoid the saturation of the amplifiers when the pixel output voltage is large, an adaptive-gain technique is used. The gain of 1 or 8 is adapted to the sensor output depending on its amplitude. If the sensor output is less than one-tenth of the saturation level, the gain of 8 is adapted to enhance the sensitivity and to reduce the total read noise. Otherwise, the gain is set to 1. Though a similar technique is used for a high-dynamic range CMOS image sensor using 3Tr. pixels to enhance the range to high light level [4], it does not intend to enhance low light level performance because the reset noise becomes a dominant random noise source even though the random noise of readout circuits is reduced.

Figures 2 and 3 show the circuit schematics of the adaptive-gain column amplifier and the operation-timing diagram, respectively. The gain is set by the ratio of the input capacitor (8C) to the feedback capacitor (1C or 8C). The reset level of the sensor output is first sampled at the input capacitor (8C). Before the control signal TX opens the transfer gate of the pixel, the switch controlled by ϕ_2 is turned off to separate the

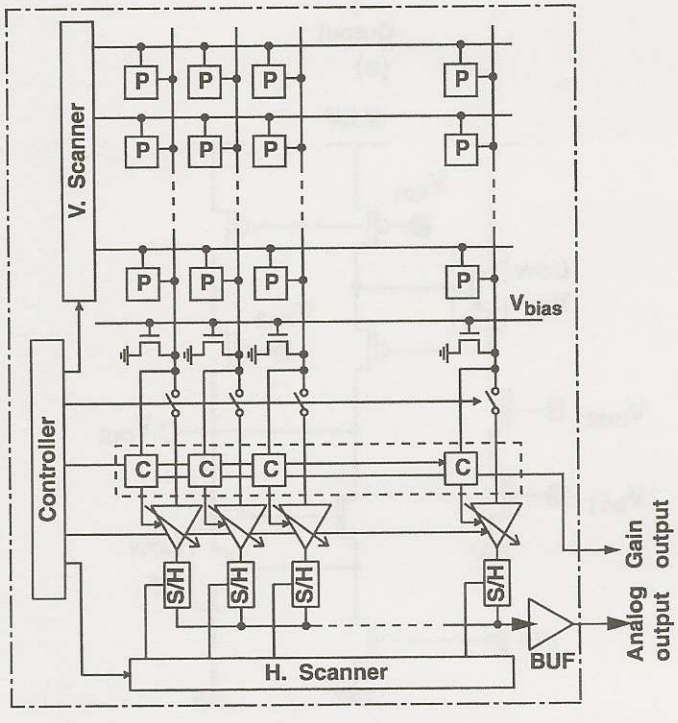
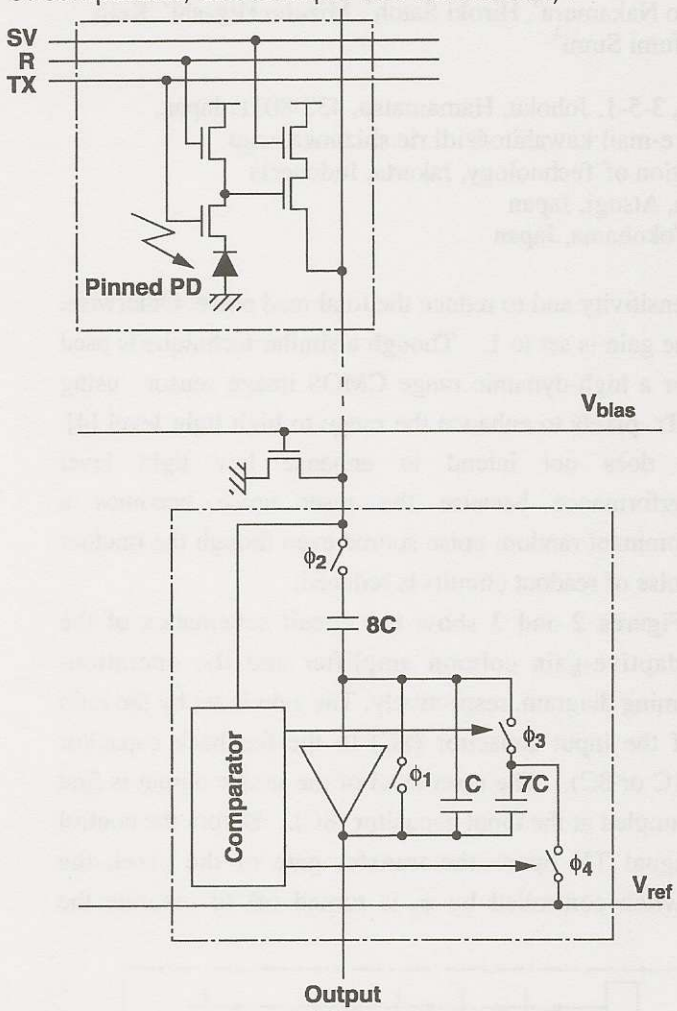
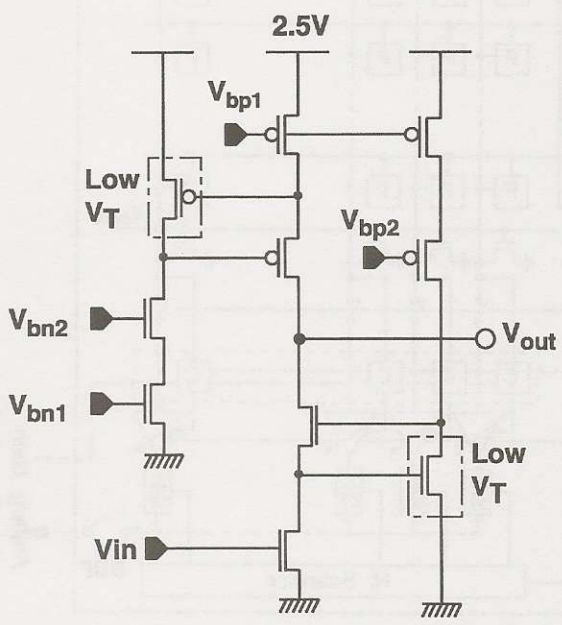


Fig.1 Block diagram of the sensor chip(P: pixel, C: comparator, S/H :sample-and-hold circuit) .



(a)



(b)

Fig.2 (a) gain-adaptive column amplifier
(b) gain-boosted cascode amplifier.

input capacitor from the sensor output. The signal level appeared at the sensor output when the transfer gate is opened is first given to the comparator and is compared with a reference voltage. The reference voltage is chosen as a little smaller level than one-eighth of the saturation voltage of the sensor output, so that the precision comparators are not necessary. The amplifier output is given by

$$V_{OUT} = \begin{cases} 1\times(V_R - V_S) + V_{OS} & (V_{R0} - V_S > V_T) \\ 8\times(V_R - V_S) + V_{OS} & (V_{R0} - V_S \le V_T) \end{cases}$$

where V_R and V_S are the reset level and the signal level of the pixel output, respectively, V_{OS} the short circuit voltage of the amplifier, V_{RO} the common reset level, and V_T the threshold voltage. Hence the column amplifier works as a correlated double sampling circuit and the reset noise and fixed pattern noise are cancelled. Since the comparators use the common reset level, the fixed pattern noise due to the pixel transistors influences to the comparison level at the comparators. However, by choosing the threshold level of the comparator to be a sufficiently small value compared with the one-eighth of the full scale of the column amplifier, and using a large gain internal amplifier in the column amplifier, the influence of the fixed pattern noise to the final output can be removed.

The decision results of comparators are read out as one-bit digital code of the applied gain, and are also used for gain setting at the column amplifiers. The amplified signals with their individual gain are sampled and held for horizontal scanning.

One of possible problems in 4-transistor active pixel circuits with in-pixel charge transfer is the reduction of saturation voltage. This paper introduces a technique to increase the saturation voltage using a proper timing of the pixel selection signal SV, which is raised a little later than the falling edge of the reset control signal R. This bootstraps the reset level of the floating diffusion node to higher voltage, and the resulting saturation voltage is enhanced to 1.0V.

The precision of the digital correction method is deteriorated if the analog interface circuits have non-linear response. To achieve the high linearity in the

switched capacitor column amplifier, the open-loop gain of the amplifier have to be large enough. The designed gain-boosted cascode amplifier shown in Fig. 2(b) has the open-loop gain of 96dB. MOS transistors with the low threshold voltage transistors are partially

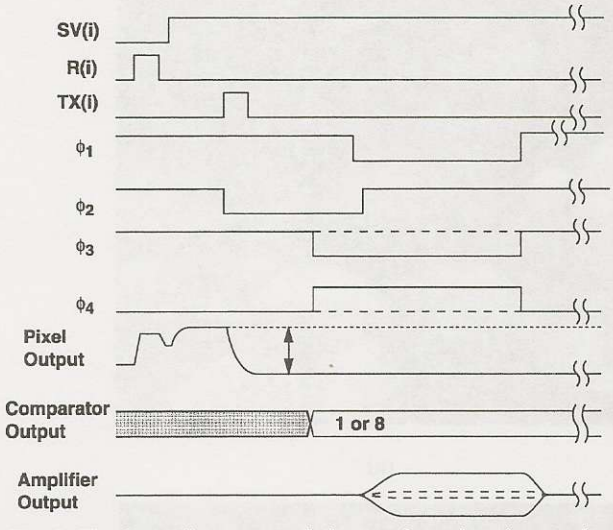


Fig.3 Timing diagram of the gain-adaptive column amplifier.

used to attain sufficient linear range of 1.1Vp-p with 2.5V supply voltage.

3. DIGITAL FPN CANCELLATION

The use of high-gain column amplifiers causes fixed-pattern noises of vertical stripes due to the offset and the gain deviations. The fixed pattern noise is removed with the circuits shown in Fig. 4. The gain and the offset deviations are measured with the zero input and a constant voltage for both gains of 1 and 8. The corrected output Y_c is given by

$$Y_c = Y(1 - E_G) - E_O$$

where Y is the output before the correction, E_o is the offset correction coefficient and E_G is given by

$$E_G = \Delta G / G$$

with the gain G and the gain deviation ΔG. The gain correction coefficients E_G and the offset correction coefficients E_O for the gains of 1 and 8 are memorized in four 1H (364) memories.

The 1-bit gain code is used for the switching of offset and gain coefficients and for shifting 3 bits if the gain of 8 is adapted to the corresponding pixel output. The resulting digital dynamic range is 17bits. Because of this high digital dynamic range, a programmable gain amplifier, which is commonly used in front of the ADC, is unnecessary. Furthermore, all the image signal processing can be done in the digital domain without degradation of the SNR.

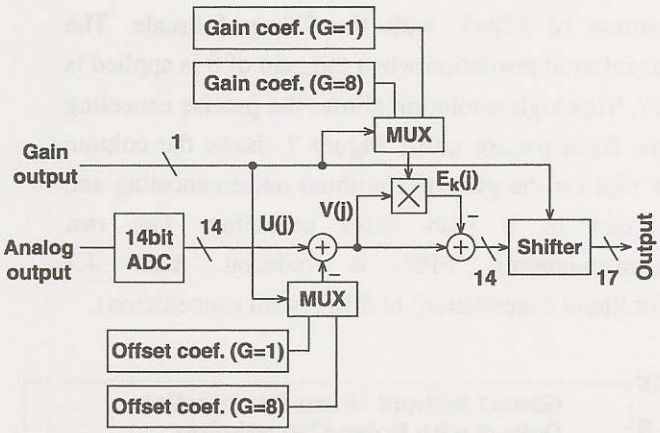


Fig.4 Digital correction of offset and gain of the column amplifiers.

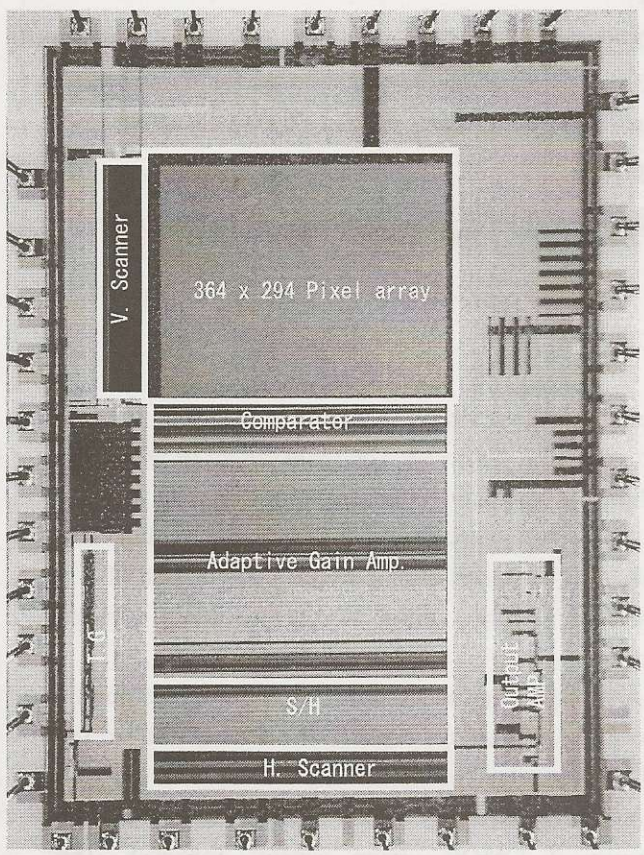


Fig.5 Chip photograph.

4. RESULTS

A CIF-size image sensor chip with the area of 4.3(H) mm x 5.0(V) mm is fabricated in 0.25μm triple-metal double-poly CMOS with a pinned photodiode technology (Figure 5). The analog sensor output is digitized using a 14bit 10MSps ADC which has a resolution of 122μV with the 2Vp-p fullscale. The input-referred resolution when the gain of 8 is applied is 15μV. This high resolution allows the precise canceling of the fixed pattern noise. Figure 7 shows the column FPN plot for the gain of 1 without noise canceling and the gain of 8 with noise canceling. The rms column-to-column FPN is reduced from 1.7 mV(without cancellation) to 50μV(with cancellation).

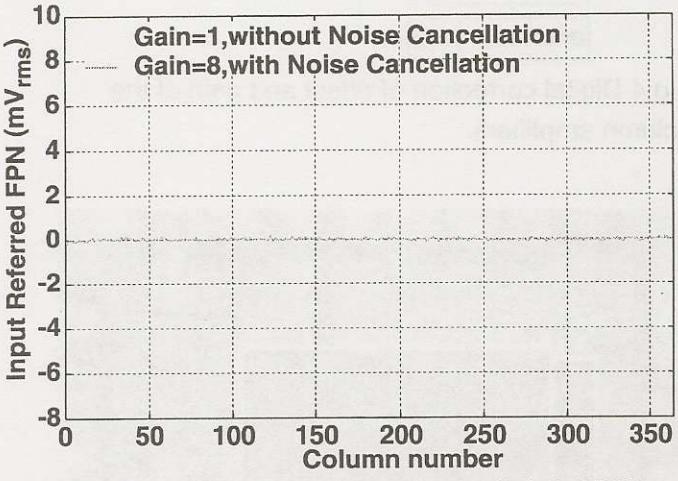
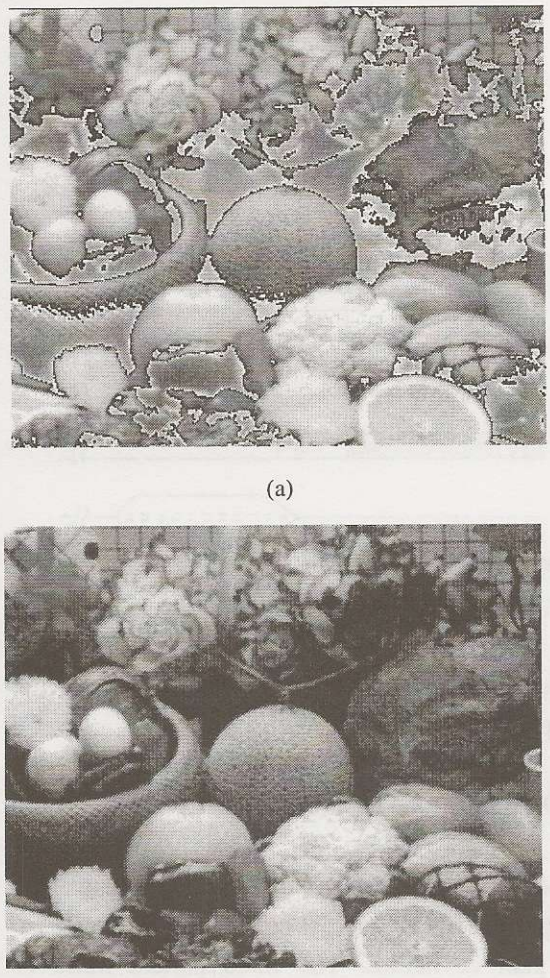


Fig. 6 FPN plot with and without digital FPN cancellation.

A sample image is shown in Fig. 6. In Fig. 6(a), the raw analog output is observed. The pixel output of which the amplitude is less than 100mV is amplified with the gain of 8. Therefore, dark region is shifted to a brighter side. In Fig. 6(b), the pixel output amplified by a gain of 8 is divided by 8 in the digital domain to attain a linear response.

Table I shows the performance summary. The pinned photo diode technology reduces the dark current to the level of the CCD. The random read noise with the gain of 8 is sufficiently small compared with the conventional CMOS image sensors reported. The calculated random readout noise due to the readout signal chain including the pixel source follower, the column switched capacitor amplifier and the sample and hold circuits is much smaller than the measurement results. The crosstalk noise components may affect to the total noise, and these can be further reduced by the design optimization of circuits and timing.



(a)

(b)

(a) Raw image (without gain correction)
(b) Reconstructed image (with gain correction)

Fig.6 Sample image.

5. Conclusiotns

This paper presents a CMOS image sensor with gain-adaptive amplifiers at the column. The totally low-noise characteristics have been demonstrated. The further reduction of the noise level is left as a future subject, since the noise calculation results suggest that the possibility of the random read noise of less than 100μV$_{rms}$.

Table I Performance Summary..

Technology	**0.25 μm CMOS 2P3M**
Chip size	**4.3(H) mm x 5.0(V) mm**
Array size	**364 x 294**
Pixel size	**4.95 x 4.95 μm^2**
Sensitivity	**3.9V/lx·s (Gain=1)**
Random noise	**263μV_{rms} (Gain=8)** **785μV_{rms} (Gain=1)**
Fixed pattern noise	**50μV_{rms} (Gain=8)**
Dark current	**18mV/s (@60°C)**
Saturation signal	**1.0V**
Dynamic range	**71dB**
Power suppy	**2.5V single**
Power consumption	**33mW**

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