

Dark Current Characterization of the CMOS APS Imagers with Test Patterns Fabricated Using a 0.18 μm CMOS Technology

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Abstracts - The characteristics of dark currents have been investigated in the CMOS APS with test patterns fabricated with the 0.18 μm CMOS technology. We found that the peripheral contribution of the photo-diode is the dominant source of dark currents in our pixel structure, and this factor is very sensitive to the distance between the surface of the STI and the n-type region of the photo-diode. Dark Currents from the transfer gate can be effectively reduced by the p^+ region on the surface of the structure, and those from the floating diffusion node were estimated as the negligible value in the normal operational mode. However, because of the enhanced thermal generation velocity caused by the severe process-induced damages, the floating diffusion node was estimated as the main source of increased dark currents in the single frame capture mode.

I. Introduction

CMOS active pixel sensors (APS), fabricated using a standard CMOS process, have advantages of low power consumption, low cost and high levels of integration [1]. Due to intensive works for past several years, CMOS APS imagers are now considered as a viable alternative to CCDs in many application fields. However, the dark current levels reported for CMOS APS imagers in current technologies are still more than an order of magnitude larger than those of the CCD sensors with the optimal fabrication process [2].

Dark currents reduce the charge capacity dedicated for photo-carriers. Moreover, this current component varies with the sensor location and time, producing the spatial and temporal variation of the output signals. The spatially varying part contributes to the fixed pattern noise of the imager and the temporal part is one of the sources for random noise, which is called the dark current shot noise [3].

As the CMOS technologies are downscaled to deep sub micron eras, it becomes more difficult to fabricate the low dark current imagers because of the processes of shallow trench isolation (STI), silicide, and shallow source/drain junction etc, which were developed for the efficient logic/mixed-mode circuit operation in the deep sub-micron CMOS technology. To implement the low dark current CMOS APS with a deep sub-micron technology, it is very important to find out where the dark currents are coming from and what types of currents they are. In this paper, we analyzed the sources and characteristics of dark currents in the 4-transistor type CMOS APS fabricated using a 0.18 μm CMOS technology. Several test patterns and modified operational clocks were used to find out the sources of dark currents. The dominant mechanisms of dark currents generated from each region of the APS structure were also estimated using the thermal activation energy computed from the temperature dependent characteristics of dark currents.

II. Pixel Type Test Pattern Structure

Fig. 1 shows the approximate cross-sectional view of the test structure of 4-transistor type active pixel [3], [4]. In this test structure, the p^+ region on the surface of the structure is used to reduce the dark currents. The p^+ region on the surface suppresses the noise caused by the interface traps located in the surface of the pixel structure. The sidewalls and edges of the STI, which have been known as the main sources of junction leakage currents, are surrounded by the p-well region. As the doping density of the p-well region is relatively higher than that of the n-type region of the photo-diode, the sidewalls and edges of the STI can be isolated from the depletion region during the integration time. The notation d_1 in Fig. 1 represents the distance between the STI sidewalls and the photo-diode on a mask patterning size. By using the low noise pixel structure of Fig. 1, dark currents can be suppressed significantly. However the residual dark currents still exist and the sources of them can be classified into several regions such as the bulk and periphery of the photodiode (PD), the photodiode/oxide interface, the charge transfer gate (TG), and the floating diffusion node (FD), etc.

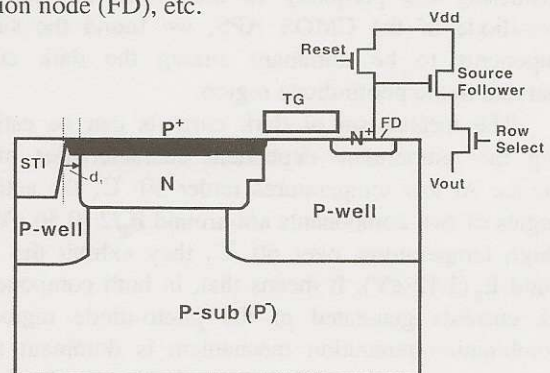


Fig. 1. The cross-sectional view of the test structure of 4-transistor type active pixel.

III. Results and Discussion

A. Photo-diode Region

The photo-diode of the proposed pixel type CMOS APS test pattern has the structure of p+/n/p- triple layers, which are isolated by the STI. The dark currents generated from this region can be classified into the area and periphery components. The area component includes the dark currents from the depletion region of p-n junction in the bulk and at the surface. The injection-diffusion currents in the bulk and "defect-generated" dark currents caused by heavy metals, crystal defects, etc. can be included in this component. The periphery component is deeply related to the defective sidewalls and edges of the STI. As mentioned earlier, in the proposed pixel structure, the sidewalls and edges of the STI are separated from the depletion region by the p-well, which has a relatively high doping density. As the distance between the surface of the STI and the n-type region of the photo-diode increases, the dark currents induced by the defective sidewalls and edges can be reduced. However, as the some characteristics of the CMOS APS, such as the photosensitivity and the saturation level are degraded with the increase of the distance, the distance between them should be determined with care.

Fig. 2 shows the bulk and periphery components of dark currents extracted from the measurements of large area test patterns at various temperatures with the reverse bias of 2.8 V. The large area square diodes were designed to monitor the dark currents due to the bulk and surface of the photo-diode, and the long periphery finger type diodes were designed to measure the dark currents due to the sidewall junctions. From the results of Fig.2, it can be shown that the dark currents generated from the sidewall regions are much higher than those from the bulk and surface regions. The peripheral components ($d_1 = 0.1 \mu\text{m}$) per unit length are about 1.9~3.6 times larger than the area components per unit area. It means that the surface dark currents of the photo-diode, which are belonged to the area components, can be successfully suppressed by the passivation of the traps at the Si/SiO₂ interface with the pinning implantation. Considering the periphery to area ratio of 1.8 in the photo-diode of the CMOS APS, we found the sidewall components to be dominant among the dark currents generated in the photo-diode region.

The mechanism of dark currents can be estimated using the temperature dependent characteristics of dark currents. At low temperatures under 50 °C, the activation energies of two components are around $E_g/2$ (0.56 eV), and at high temperatures over 60 °C, they exhibit the values around E_g (1.12 eV). It means that, in both components of dark currents generated in the photo-diode region, the recombination-generation mechanism is dominant at low temperatures and the diffusion mechanism is dominant at high temperatures.

Fig.3 shows the variation of peripheral components of the dark current for different distances between the surface of the STI and the n-type region of the photo-diode.

From Fig.3, it can be shown that the dark currents due to the sidewall junctions are sensitive to the distance between them. The peripheral component of dark currents with the distance $d_1 = 0.0 \mu\text{m}$ is about 1.2 times larger than that with the $d_1 = 0.1 \mu\text{m}$, and the peripheral component of dark current with the distance $d_1 = 0.2 \mu\text{m}$ is about 0.57 times larger than that with the $d_1 = 0.1 \mu\text{m}$ at 60 °C. The sidewall junction leakage currents that are characterized by the patterns without STI shows 0.25 times larger than that with the $d_1 = 0.1 \mu\text{m}$. It means that the dark currents related to the defective sidewalls and edges of STI are roughly 75 % of the peripheral components for the $d_1 = 0.1 \mu\text{m}$ device at 60 °C.

The dark currents due to the sidewall junctions increase dramatically when the p-well region is eliminated. The peripheral component of dark currents with the distance $d_1 = -0.1 \mu\text{m}$ is about 13 times larger than that with the $d_1 = 0.1 \mu\text{m}$, and the peripheral component of dark currents without the p-well region is about 47 times larger than that with the $d_1 = 0.1 \mu\text{m}$ at 60 °C. In these cases, the enhanced thermal generation follows from the creation of interface traps caused by the defective sidewalls and edges, and it can be verified by the activation energies of 0.80 eV and 0.67 eV, which are close to $E_g/2$ even at high temperatures.

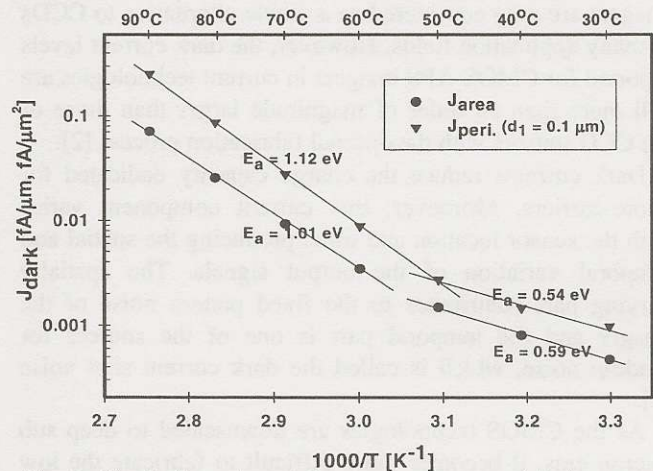


Fig. 2. The bulk and periphery components of dark currents generated in the photo-diode, which are extracted from the measurements of large area test patterns at various temperatures. Dark currents from the sidewall regions are much higher value than those from the bulk and surface

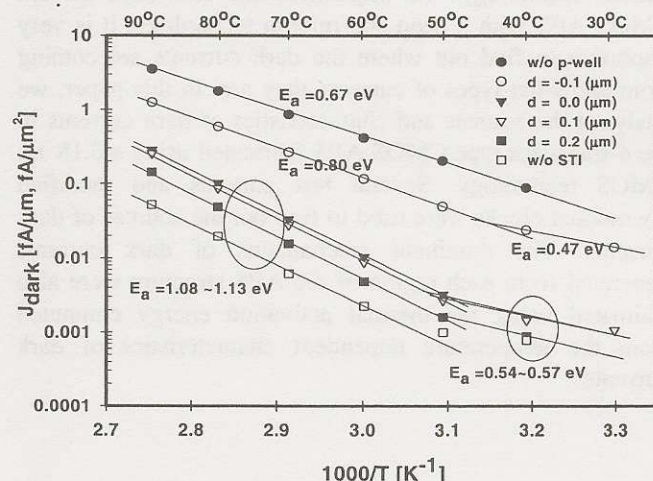


Fig. 3. The variation of peripheral components of the dark currents for different distances between the surface of the STI and the n-type region of the photo-diode. It can be shown that the dark currents due to the sidewall junctions are sensitive to the distance between them.

B. Transfer Gate Region

The transfer gate means the MOSFET, which transfers the signal charges from the photo-diode to the floating diffusion node.

To investigate the dark currents related with the transfer gate, the dark currents from the CMOS APS are characterized and compared with those from the photo-diode which are calculated from the characterization results of Fig.2 by the equation of

$$\frac{\Delta V}{\Delta t} \left(\frac{V}{s} \right) = (J_{\text{area}} A_{\text{diode}} + J_{\text{peri}} L_{\text{diode}}) \times \frac{G_{\text{SF}}}{C_{\text{FD}}} \left(\frac{A}{F} \right)$$

where ΔV is the voltage drop due to dark currents, t is the integration time, J_{area} is the area component per unit area, J_{peri} is the periphery component per unit length, A_{diode} is the photo-diode area in the CMOS APS, L_{diode} is the length of the photo-diode periphery in the CMOS APS, C_{FD} is the capacitance of the floating diffusion node, and G_{SF} is the gain of the source follower.

From the results of Fig.4, it can be shown that the generated dark currents show the comparable value with those from the photo-diode. It means that the dark currents generated from the transfer gate can be suppressed successfully with our pixel type test structure. It seems that the tail of the p+ region on the surface of the photo-diode can passivate the interface traps on the surface of the transfer gate without the severe degradation of the charge transfer characteristics in the CMOS APS.

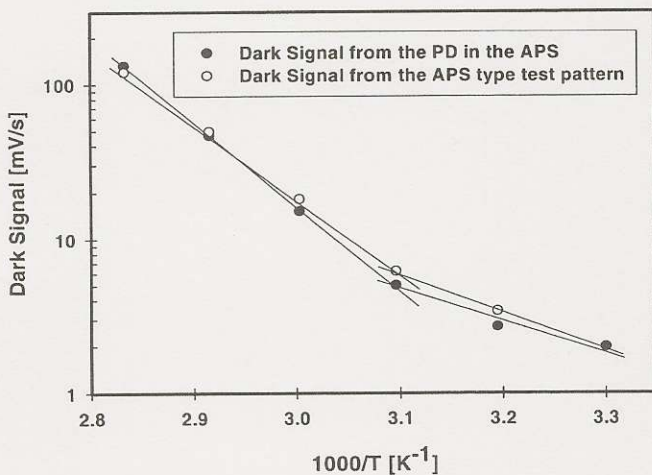


Fig. 4. The comparison of dark currents generated from the photo-diode and those from the APS type test pattern.

C. Floating Diffusion Node Region

The floating diffusion node (FD) means the region where the integrated charges are converted to the voltage.

Generally, as the integration time in the floating diffusion node is very short (about several μs) in the normal operation mode, this region is not considered as the main source of dark currents in the 4-transistor type CMOS APS. However, because of the severe process-induced damages that are caused by the contact etching process and the high dose implantation, etc., the generation velocity in the depletion region of the n-p junctions can be enhanced. Moreover, in the operation of the single frame capture mode [5]-[6], the integration time in the floating diffusion node increases to about 1/30 s, so this region can be the main source of the CMOS APS in this operation mode.

In our experiments, the modified operational clock is used to investigate the dark currents related with the floating diffusion node region. After the integration of the dark-electrons only in a floating diffusion node for 1/30 s, the output signals are characterized at various temperatures. Fig. 5 shows the dark signals generated in the floating diffusion node for the integration time of 1/30 s. From this result, it can be shown that the dark signals generated in the floating diffusion node are much higher than those from the photo-diode or the transfer gate if integrated for the same time of 1/30 s. At 60 °C, the magnitude of dark signal is about 1100 mV/s, which is about 40 times larger than that of the CMOS APS with the $d_1=0.1 \mu\text{m}$. The activation energy calculated from the temperature dependent characteristics of dark signals shows the value of about 0.6 eV at all temperatures from 30 °C to 80 °C. It means that the dominant mechanism of the dark signals generated in the floating diffusion node is the generation-recombination, which is deeply related with the process-induced damage.

From this result, it can be confirmed that the thermal generation velocities in the floating diffusion node are much higher than those from the photo-diode and the transfer gate region in our pixel structure, and this region can be the cause of increased dark currents in the single frame capture mode. However, as the integration time in this region is only about 1/10000 of that in the photo-diode and the transfer gate, the dark currents generated from the floating diffusion node can be estimated as a negligible value (under 1/100 of the overall dark currents from the CMOS APS) in the normal operational mode.

