High Burst Rate CCD's Capable of Imaging at 1-5 Million Frames Per Second

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Abstract

This paper describes the architecture, process technology, and performance of a family of high burst rate CCDs. These imagers employ high speed, low lag photo-detectors with local storage at each photo-detector to achieve image capture at rates greater than 10^6 frames per second. The first imager has 64 x 64 spatial resolution with 12 frames of storage. The second imager has 80 x 160 spatial resolution with 28 frames of storage. The third imager has 64 x 64 spatial resolution with 312 frames of storage.

I. Introduction

A family of ultra high frame rate charge coupled device (CCD) image sensors and cameras have been developed capable of image acquisition frame rates > 1 million frames per second. The image acquisition frame rate is the rate at which photoelectrons are read out of the photo-detector into the pixel's memory array. After the pixel memory fills, further exposures replace the oldest stored images in a "first in-first out" mode of operation.

Thus the imager continuously stores the latest images acquired. This allows a pre-trigger mode of operation, making it possible to capture poorly predicted and spontaneous transient events. Readout of the stored images is similar to a frame transfer CCD readout and is at a comparatively slow pixel rate, consistent with low readout noise and inexpensive, PC based camera data acquisition systems. During the readout, the images are demultiplexed and assembled in the computer's memory for display.

These high burst rate cameras have been developed to capture scientifically useful digital image data of high speed transient events where microsecond temporal resolution is required. Application areas include capture of rapid mechanical motion, wavefront sensing, fluid cavitation research, combustion studies, plasma research and wind-tunnel-based gas dynamics research.

II. Theory of Operation

The high burst rate imagers combine a high speed, multi-implant (graded) pinned-buried photo-detector with local buried n-channel CCD storage elements at each macropixel. A typical cross-sectional view of the photo-detector and readout gates is shown in Figure 1. The various designs implemented to date employ a variety of local storage configurations. Figure 2 shows an example of a serial-parallel architecture. This architecture is employed on the 64 x 64 imager with 312 storage elements per macropixel. The typical construction and operation of the photo-detector readout is shown in Figure 3.

During charge accumulation, the photocharge is swept into the G1 collecting well by the stepped potential profile. Anti-blooming is provided by a lateral overflow drain formed by G2 and V_{DR}. The oldest image sample is transferred to a drain via the path S1 to V_{DR}, in the typical configuration.

During frame readout, the G1 gate is turned off to isolate the photo-detector from the local frame storage. The frame storage stages are then clocked to one or two horizontal register(s) which have one to four (depending upon the design) floating-diffusion source follower outputs.

III. Process Technology and Design

The high burst rate imagers are fabricated on p-type EPI. The new generation of CCDs employ three levels of polysilicon for two of the designs, with a fourth level of polysilicon added for the 312 storage element macropixel design. Two levels of metallization are utilized. Up to seven photo-detector implants are employed.

A major challenge in manufacturing these CCDs is attaining high yield given the severe topology of the small storage element designs. Modifications to the standard processing have proven successful in improving, in particular, the metal level yields.

Storage elements as small as 5.5 µm x 4.5 µm were previously demonstrated.[1] The new designs employ a storage element size of 6.7 µm x 6.5 µm. All designs employ customized implants to maximize charge handling capacity.

IV. Testing Results

All three of the new designs have yielded operational imagers, producing high speed imagery in their respective camera systems.

The most comprehensive data has been taken on the 64 x 64 spatial resolution imager with 12 frames of storage. Table 1 summarizes the measured performance. The net quantum efficiency is the product of the fill-factor and the reported QE.

Table 1: 64 x 64 Design

Format	64 x 64 x 12 frames
Macropixel Pitch	116 µm x 116 µm
Optical Fill-Factor	50%
Quantum Efficiency:	
255 nm	36%
430 nm	46%
660 nm	45%
880 nm	21%
Maximum Frame Rate	5×10^6 fps
Full Well	30,000 e
Noise Floor	30 e RMS

Figure 4 shows twelve frames of imagery in which frames 1, 4, and 10 were exposed by 50 nsec pulses of light. The images were acquired at 5 million frames per second. There is a 5% trailing image, due primarily to the time constant of the photo-detector. Figure 5 indicates the intensity of the trailing image as a function of the time between the end of the light pulse and transfer of the photoelectrons into the charge storage memory.

V. Conclusions

A new family of high burst rate imagers and cameras have been demonstrated. All are designed to operate at > 1 million frames per second. The 80 x 160 spatial resolution (28 frames of storage) and 64 x 64 spatial resolution (312 frames of storage) imagers are three side buttable to permit assembly of higher resolution mosaic focal planes. The fastest imager, the 64 x 64 spatial resolution (12 frames of storage) CCD, has operated successfully at 5 million frames per second.

VI. Acknowledgement

The authors acknowledge the original, innovative design work performed by Dr. Walter F. Kosonocky. Dr. Kosonocky developed the original conceptual architecture for the high burst rate CCD and lead the design team which demonstrated the earlier versions of these devices[1].

VII. References

1. Walter F. Kosonocky et.al., "360 x 360 Element Three-Phase Very High Frame Rate Burst Image Sensor: Design, Operation and Performance", IEEE Trans. Electron Devices, Vol ED-44, pp. 1617-1624, 1997.

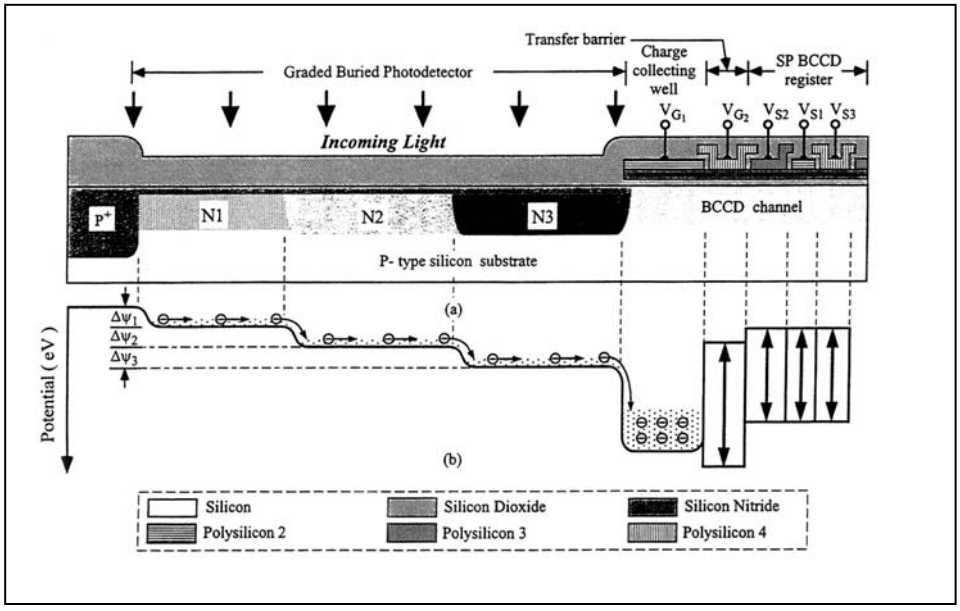

Figure 1. (a) Typical cross-sectional view illustrating the photo-detector doping. (b) Corresponding potential distribution.

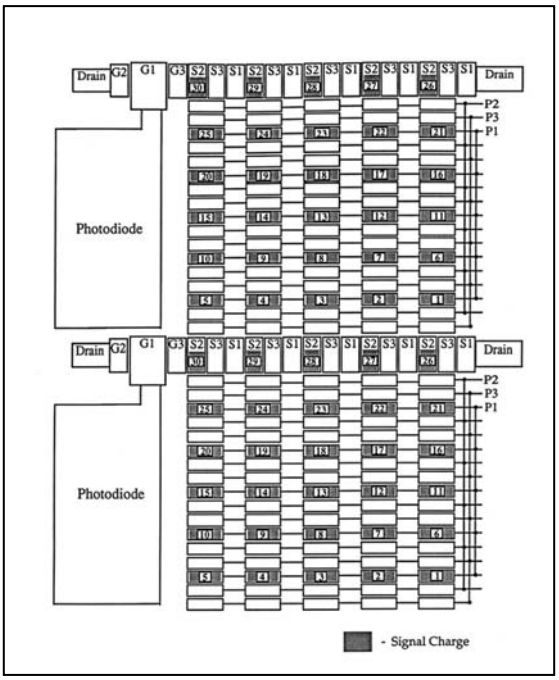

Figure 2. Example of macropixel architecture with buried channel CCD storage. Both serial-parallel and serial storage registers employed in the new designs.

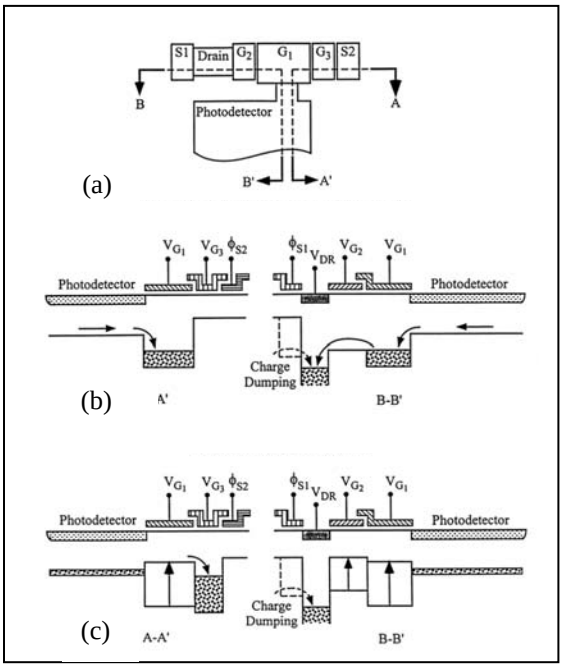

Figure 3. Typical construction and operation of photo-detector readout. (a) Top view of the photo-detector output structure. (b) Cross section of *A-A*^{1} and *B-B*^{1} and potential profiles during the charge accumulation. (c) Cross section of *A-A*^{1} and *B-B*^{1} and potential profiles during the charge readout.

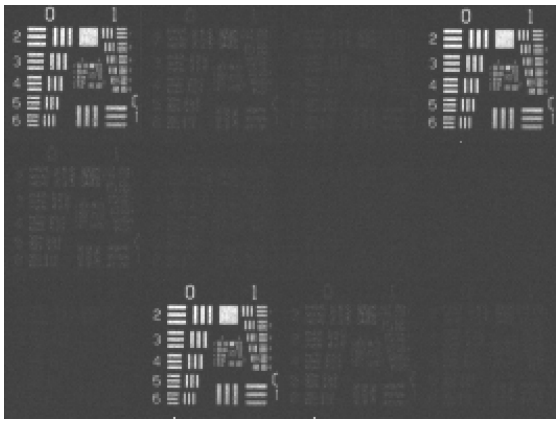

Figure 4. Twelve consecutive frames of data from the 64 x 64 high burst rate camera. Imagery taken at 5 million frames per second.

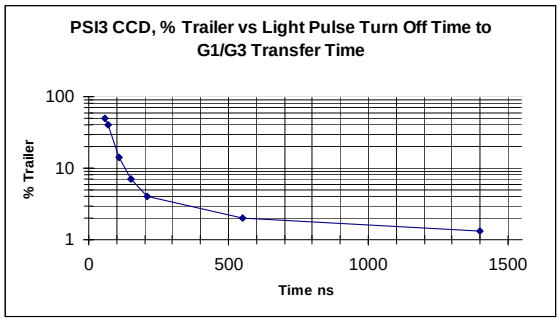

Figure 5. Measured trailer as a function of delay from light pulse to photo-detector readout.