Enhanced Full Well for Vertical Antiblooming, High Sensitivity Time-Delay and Integration (TDI) CCDs with GHz Data Rates

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Abstract

The authors present a novel pixel for use in vertical antiblooming (VAB) CCD structures. This novel pixel increases the charge handling capacity of VAB pixels, without unduly compromising VAB performance. This is corroborated with simulations and experimental data as demonstrated on GHz data rate Time-Delay and Integration CCD imagers. Tradeoffs of using this pixel structure are also highlighted.

I. Introduction

Time-Delay and Integration (TDI) Charge-Coupled Device (CCD) image sensors continue to find widespread application in many industrial imaging applications, where high speed and superior image quality are primary requirements [1]. The use of TDI, based on integrating an image across multiple pixel rows (TDI stages), provides for an increase in the collected signal as compared to a conventional single-row linescan CCD.

To avoid loss of information from an image with bright highlights, the pixels can be designed to provide a level of anti-blooming performance using Vertical or Lateral Anti-blooming structures [2-4]. However, both can reduce the charge storage capacity of the pixel. This in turn reduces the CCD dynamic range

We have developed a VAB pixel that solves this problem and allows high full well capacities to be achieved. Here, we describe how the use of two adjacent gaps in the p-well implant mask, in conjunction with the p-well thermal diffusion, can form an increased-width VAB structure for enhanced full well without sacrificing VAB performance.

II. The Theory of Operation

Figure 1(a) shows a pixel layout and cross section for a conventional VAB pixel. With this conventional VAB pixel, the CCD channel is formed by the buried channel implant and diffusion of a p-well implant across a gap in the implant formed by lithography, to form a lower-doped p-region in a more highly-doped p-well. If the gap is made narrower, the p-doping of this region increases. This has the effect of increasing the charge handling capacity of the pixel but in turn lowers the level of vertical antiblooming of the pixel. Conversely, if the gap is made wider, the level of p-doping decreases. This lowers the charge handling capacity of the pixel, but it increases the vertical antiblooming performance. Some adjustment in charge handling capacity can be achieved during CCD design by varying the width of the p-well gap on the photomask, and during CCD operation by adjusting the n-substrate voltage. But, for a given wafer fabrication process, large increases in the charge handling capacity of a pixel cannot be realized without decreasing antiblooming performance.

Figure 1(b) shows the layout and cross section of the novel pixel. Instead of a single gap in the p-well photomask, we implement two gaps separated by a narrow stripe of p-well between them. By proper adjustment of the width of these gaps and the width of the p-well stripe between them, the net effect is that the diffusion of the p-well implant creates a wider CCD channel as compared to the case with a single p-well gap. This increases the charge handling capacity of the pixel without impacting VAB performance.

Figure 2(a) shows a semiconductor device simulation of a single-gap structure, with a p-well gap (on the photomask) of 4 microns. The potential distribution in the substrate is plotted for Vgate=10V and Vn-substrate=16V. Figure 2(b) shows the potential distribution of the novel pixel under the same biasing and processing conditions. For this pixel, the gaps (on the photomask) are each 3.5 microns wide, separated by a 3 microns p-well stripe.

With these structures, we find that the simulated charge handling capacity of the double-gap structure is roughly ≥ 2x of that of the single-gap structure. Specifically, for a four-phase 16 x 16 micron CCD the predicted storage capacities are 584,000 e- and 240,000 e- for double and single gap structures respectively.

III. Testing and Measurements

A double-gap pixel structure was implemented on a 16 x 16 micron pitch TDI CCD sensor, with 512 TDI stages and a resolution of 2048 pixels horizontally; as well as a 13 x 13 micron pitch TDI CCD sensor with 96 TDI stages and a resolution of 4096 pixels horizontally. High speed operation is achieved through massively parallel output structures. The HCCD readout register is segmented [2] into 64 output taps per side (bi-directional scanning) of the array to allow for GHz pixel data rates [3]. The fabricated CCDs have demonstrated more than 200x vertical antiblooming (VAB) performance based upon the doubling in diameter of an over-illuminated spot whose height is 10% that of the array; the specific value depending on the particular Vn-substrate bias used. Note this antiblooming measurement was made in area array mode (where the vertical CCD clocks are held constant for a period of time, to integrate photocharge, then clocked to transfer charge to the horizontal CCD). This is opposed to TDI mode (where the vertical CCD clocks continuously shift charge across the array to the horizontal readout CCD) which is the usual mode of operation of these devices.

A schematic diagram of the sensor is illustrated in Figure 3. Features and experimental results are summarized in Table I.

Two design splits were fabricated, a version with a single gap pixel (4 microns) and a version with a double gap pixel (3.5 micron gaps, 3 micron stripe). Measurements of devices from the same semiconductor wafer, one with the single-gap pixel and one with the double-gap pixel, we find that the double gap structure has a full well of ≥580,000 e- and the single gap structure of ≥270,000 e-, when operated with the same n-substrate bias (~15V) and vertical CCD clocks with 10V swing and –2V offset. This is consistent with the modeled results.

Figure 4 shows vertical antiblooming performance of the 16 x 16 micron double-gap CCD. This is a subset of an image taken in area array mode. Here a square spot, whose side length is 10% of the height of the TDI region, is over-illuminated with 200x the saturation energy. (Here we define saturation energy as the amount of optical energy required to cause the output video signal of the CCD to deviate from a linear response by 5%). Little blooming is evident since the spot's diameter has not doubled vertically or horizontally. The white streaks above and below the spot are due to frame-shift smear, since the light source is unshuttered (area mode). The diagonal black lines are diagonal metal busses which feed the CCD clock signals to the polysilicon electrodes and would not be observed during TDI operation.

One item seen on the 16 x 16 micron pitch CCD is that the double-gap structure was observed to have a lower quantum efficiency (QE) than the single gap structure, at the peak QE wavelength. For instance, with illumination at 520 nm the double-gap structure had a QE of 19.6% and the single gap structure of 20.4% at the same wavelength, with the n-substrate bias of ~15V. This difference is small but has been repeatedly measured, with experimental uncertainty ruled out. Note also that the QE is itself a function of n-substrate bias for both structures, with the QE increasing with lowering n-substrate bias.

A photograph of the actual CCD packaged devices is presented in Figure 5.

Conclusions:

The novel dual p-well gap pixel is useful for increasing the charge handling capacities of vertical antiblooming pixels, without unduly compromising vertical antiblooming performance. This is corroborated with simulations and experimental data. Nevertheless, a slightly lower peak quantum efficiency is a tradeoff of using this novel structure.

References:

[1] DALSA CCD Databook (www.dalsa.com).

[2] G.P. Weale, M.J. Kiik, E.C. Fox, C.J. Flood, and S.G. Ingram, "Anti-blooming optimization using simulations and measurements for a VAB process", 1997 IEEE Workshop on Charge-Coupled Devices and Advanced Image Sensors, paper P-14, 1997.

[3] M.J. Kiik, C.J. Flood, G.P. Weale, and S.G. Ingram, "Frame Transfer Area Array Sensor with Vertical Antiblooming and Novel Readout for

Advanced Performance", 1997 IEEE International Electron Devices Meeting, paper 8.2.

[4] G.P. Weale, C.J. Flood, and D.J. Dykaar, "A Time-Delay and Integration Image Sensor with High Speed Output Architecture" Proc. SPIE 3301, Solid State Sensor Arrays: Development and Applications II, p. 9-16, 1998.

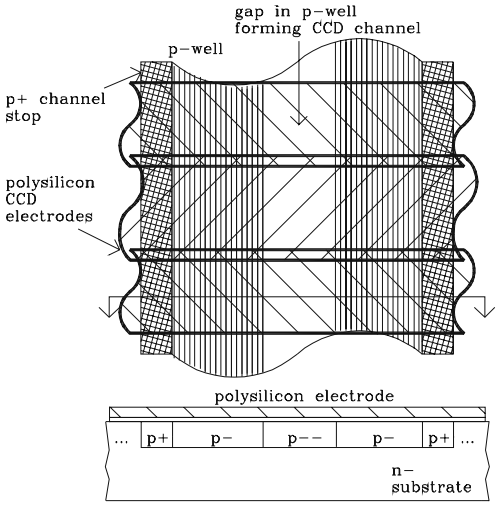

Figure 1(a) – Conventional CCD VAB Pixel layout and cross-section.

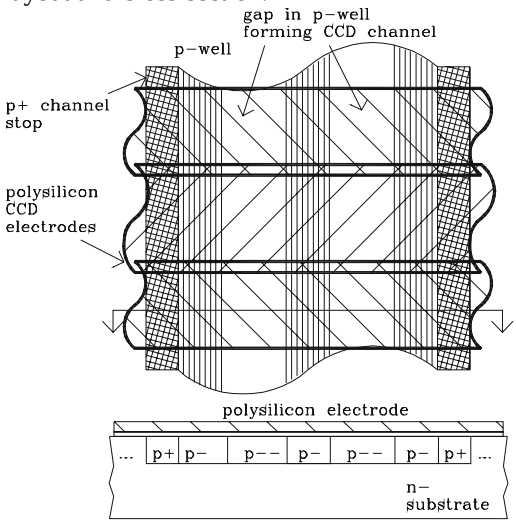

Figure 1(b) – Novel CCD Pixel layout and cross-section.

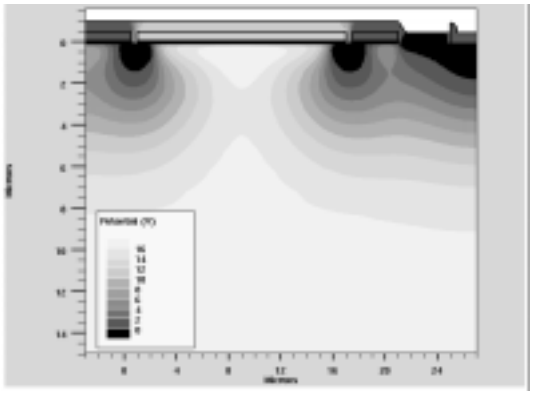

Figure 2(a) - Single gap p-well biased with Vgate=10V and Vn-substrate=16V. The structure on the right is for biasing the substrate.

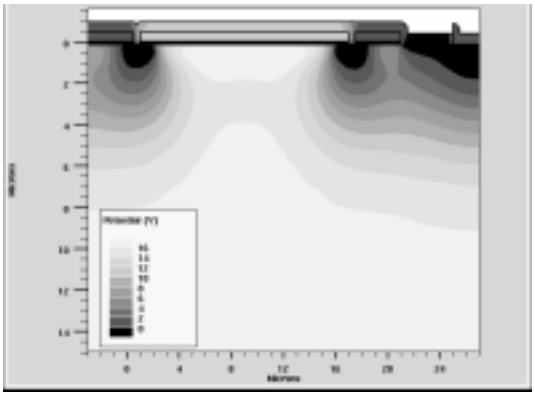

Figure 2(b) – Novel double-gap p-well structure with same biasing conditions. The CCD well is seen as having a larger area.

Table I – CCD Sensor Performance

Parameter	**Value**	
Pixel data rate (burst rate)	≥1.6 GHz (64 x ≥25 MHz)	
Pixel Size (square)	13 μm	16 μm
Full Well Signal (e-) Double-gap structure	≥220,000	≥500,000
Output Node Conversion Gain	> 5.5 μV/e-	
Anti-blooming (VAB)	> 200x based on 10% spot doubling	
Dark current (35 °C package temperature)	< 0.6 nA/cm^2	
CTE in HCCD	>0.99996 (measurement limit)	
CTE in VCCD	>0.99999	
PRNU in TDI mode	< 5% Qsat	
FPN in TDI mode	< 0.4 % Qsat	
Ch-ch uniformity	< 10% at 80% of Qsat	

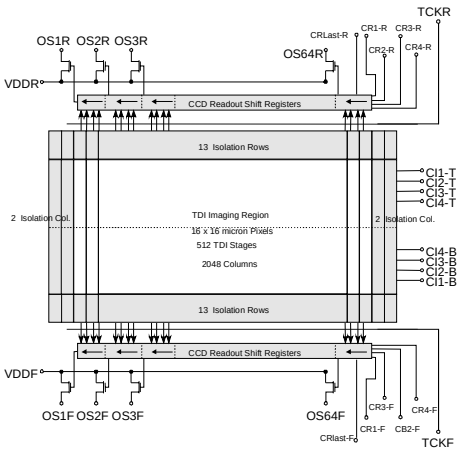

Figure 3 – GHz TDI CCD block diagram. This particular CCD is bi-directional. It has 4 vertical CCD clock phases and four horizontal CCD clock phases; the latter can be clocked in 4 phase or pseudo-two phase mode. There are 64 outputs per side.

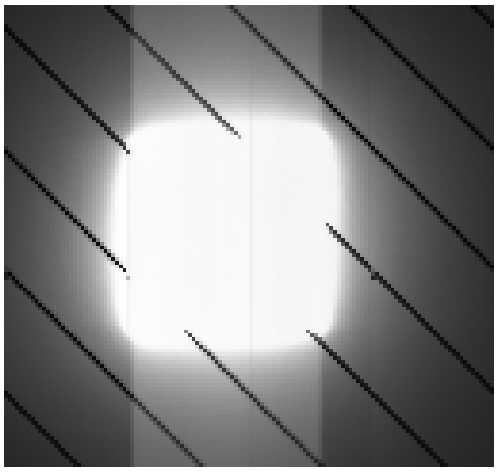

Figure 4- Vertical antiblooming performance. A square spot (whose side length is 10% of the height of the TDI region) is over-illuminated with 200x the saturation energy. The white streaks above and below the spot are due to frame-shift smear, and the diagonal black lines are diagonal metal busses which feed the CCD clock signals to the polysilicon electrodes. (These would not be observed during TDI operation). The 'bump' on the diagonal bus in the right hand side of the image is part of the bussing arrangement, and is not a cosmetic defect.

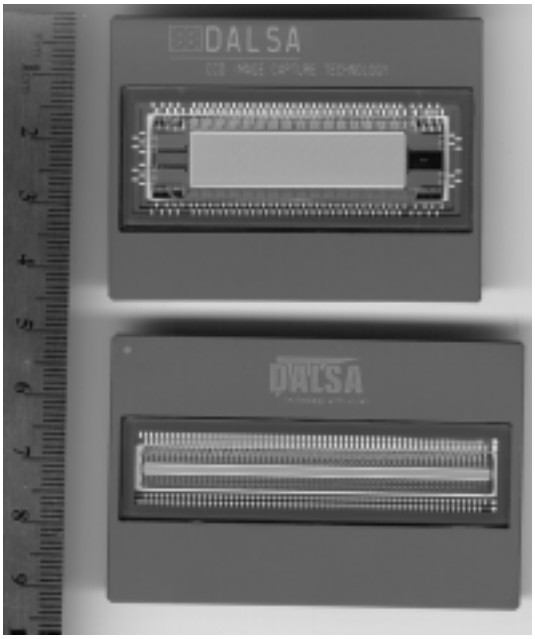

Figure 5 – The two CCD sensors. They are housed in alumina ceramic pin-grid array packages with double-sided AR coating windows. A ruler in mm is shown for comparison.