Development of CMOS Image Sensor Overlaid with a HARP Photoconversion Layer

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Abstract

With the aim of creating a highly sensitive solid-state image sensor we developed a new CMOS image sensor that was made by overlaying a HARP (High-gain Avalanche Rushing amorphous Photoconductor) photo-conversion film on to a CMOS readout circuit. Prototype sensors were fabricated using a new MOS transistor and an indium-microbump method. We developed two new connecting methods (direct-connecting and direct-evaporating) to improve the unevenness of the reproduced image, and confirmed experimentally the advantages of the direct-evaporating method.

I. Introduction

We at NHK Science and Technical Research Laboratories are continuing with our efforts to develop a CMOS image sensor overlaid with a HARP film [1] in order to produce a highly sensitive solid-state image sensor. We expect this sensor to demonstrate the following advantages when compared with the conventional CMOS and CCD image sensors.

- The large fill factor (almost 100%) and the avalanche multiplication in the HARP film enables a large signal to be obtained.
- The HARP film absorbs all incident light and therefore reduces smear.
- This CMOS image sensor does not require photodiodes, which occupy a large area in each pixel. Thus, a large number of pixels can be integrated onto the sensor.

II. Configuration and operation

A schematic diagram of the sensor and a cross-sectional view of a pixel are shown in Figs. 1 and 2. Holes generated by incident light in the HARP film are multiplied, then made to flow into the drain of an NMOS transistor, which acts as the storage diode in each pixel. Signal holes are recombined with electrons in the drain, and the potential rises with light intensity. When the scanner selects a pixel, its signal current flows into the signal line. The signal is then amplified by line amplifiers arranged in each column, while noise is reduced by a correlated double-sampling circuit to obtain a sensor output having a high signal-to-noise ratio.

III. Key technologies

Technologies for the following were needed to be able to develop this image sensor.

- Design and fabrication of a HARP film for a stacked solid-state image sensor. Our design calls for the film thickness to be 0.4 micron to get the five times avalanche multiplication when 60 V is applied.
- Increased breakdown-voltage of the MOS transistor. By virtue of a double diffused drain MOS structure, a breakdown-voltage of 60 V was achieved.
- Processes to connect the HARP film to the CMOS readout circuit.
- Noise reduction in the CMOS readout circuit.(CDS)

In this report, we describe in detail the technology used to connect the HARP film to the CMOS readout circuit.

IV. Overlaying

It is almost impossible to connect a HARP film onto a glass chip and a CMOS readout circuit because of the unevenness (maximum difference of height is 1.5 microns) of the CMOS readout circuit. Hence, it is essential that technologies for connecting the HARP film to the CMOS readout circuit be developed. We will describe the following three methods that we are currently working on (Fig. 3),

- Microbump method
- Direct-connecting method
- Direct-evaporating method

Microbump method

The main material of the HARP film is selenium, a soft non-metallic solid (metalloid) that tends to change from amorphous to crystalline with an application of heat, thus we cannot use a solder bump. Therefore, we used indium microbump electrodes to connect the HARP film to the CMOS readout circuit. Indium has a lower hardness and requires less heat to connect; thus, we could prevent any heat-related damage from occurring to the HARP film. To make the indium microbumps, we developed a lift-off-process method. We were able to form indium microbumps 9 x 9 µm and 5-µm high (Fig. 4). We used this method to construct several samples (Fig. 5).

The microbump method is relatively easy to use at the present technological level, but there have been some problems encountered, such as, unevenness and shading of the reproduced image caused by irregular bumps, warps of the surfaces, and unexpected non-parallel bonding. Since the smaller a pixel on the CMOS image sensor is, the more serious these problems are (Fig. 6), we were compelled to investigate the two methods that are described below.

Direct-connecting and direct-evaporating methods

To solve the above-mentioned problems, two new connecting methods, the direct-connecting and the direct-evaporating, were developed. The direct-connecting method is used to connect the CMOS readout circuits to the glass chip with a HARP film without using any microbumps. The direct-evaporate method is used to deposit the HARP film in inverse order onto the CMOS readout circuit. Both methods require the flattening and smoothing of the Si chip to the order of nanometers, hence, we introduced a chemical mechanical polishing (CMP) technology for the aluminum pillar process (Fig. 7).

In both methods, the required planarities are different. In the direct-evaporating method, the local planarity of the Si chip is required to be less than 10 nm, comparable to the planarity of a glass chip.

We formed aluminum pillars by using electron-beam evaporating and the lift-off process with thick photoresist layers (3-µm high). After evaporating the TEOS-ILD (SiO_2), we polished the TEOS-ILD and the aluminum pillars surfaces to prepare them for planarization. Figure 8 shows SEM images of a cross-section of the CMOS readout circuit both before CMP and after CMP. The global uniformity of the surface flatness determined by the TEOS-ILD thickness is shown in Fig. 9. In addition, we wanted to enhance the quality of the used slurry to prevent aluminum corrosion. We achieved a 10% global uniformity and a local planarity of 50 nm (Fig. 10).

We were able to achieve sufficient planarity in our experiments. We are now continuing with the development of a technique to evaporate a HARP film onto a CMOS readout circuit.

IV. Fabrication and measurement

When we applied the direct-evaporating method, the reproduced images were more even and less shaded (see Fig. 11). We used the direct-evaporating method to confirm successful planarization, but the quality of the HARP film had declined due to the inverse order evaporating. We need to further develop the inverse-order evaporating method for the HARP film as well as the direct-connection method.

V. Conclusion

We described the composition of a CMOS image sensor overlaid with a HARP photoconversion layer and the advantages of the sensor. And we described the essential technologies employed in the device, mainly the HARP-film connecting method, in detail. We also described the improvements of unevenness and shading derived from using the two new connecting methods. From now on, though we will further investigate these two methods and incorporate their technologies in image-sensor fabrication, we will continue to search for more reliable method of connecting HARP films with an aim toward higher resolution.

Acknowledgements

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References

[1] K. Tanioka, J. Yamazaki, K. Shidara, K. Taketoshi, T. Kawamura, T. Hirai, and Y. Takasaki, “Avalanche-mode Amorphous Selenium Photoconductive Target for Camera Tube, in Advances in Electronics and Electron Physics, 74, pp. 379-387, Academic Press (1988).

[2] W.D. Park, Y. Takiguchi, M. Kosugi, M. Kubota, Y. Ohkawa, K. Miyakawa, S. Suzuki, K. Shidara, K. Tanioka, A. Kobayashi, and T. Hirai, “An a-Se HARP Layer for a Solid-State Image Sensor”, in Proc. IEEE Workshop on CCD and Advanced Image Sensors, Karuizawa, Japan, 1999.

[3] M. Nakayama, H. Ohtake, M. Yamauchi, T. Tajima, and M. Abe, “A High-Voltage MOS Transistor for Solid-State Imager with Avalanche Multiplier Film”, in Proc. 1997 IEICE General Conference, C-11-10, 1997 (in Japanese).

[4] T. Hayashida, T. Tajima, M. Yamauchi, M. Kosugi, H. Ohtake, Y. Ishiguro, T. Watabe, K. Yamano, Y. Takiguchi, H. Kokubun, T. Watanabe, and M. Abe, “Process-development of CMOS Image Sensor Overlaid with a HARP Photoconversion Layer”, in Proceedings of the 2000 ITE Annual Convention, pp. 139-140 (Aug. 2000).

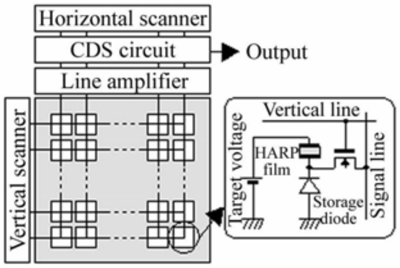


Fig. 1 Schematic diagram of the CMOS image sensor overlaid with a HARP film.

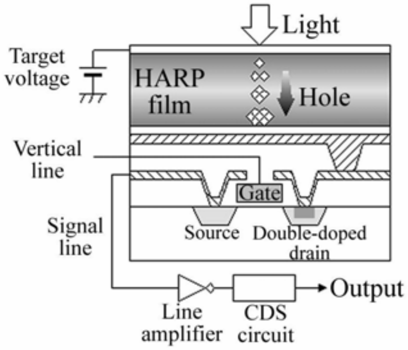
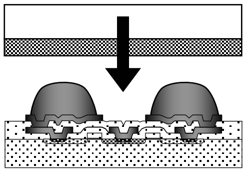
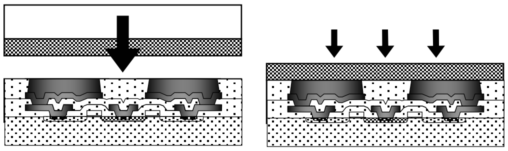


Fig. 2 Cross-sectional view of a pixel.



a) Indium microbump method



b) Direct-connecting method c) Direct-evaporating method

Fig. 3 HARP film connecting methods

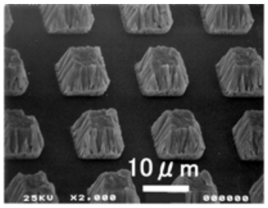


Fig. 4 Photograph of the Indium microbumps

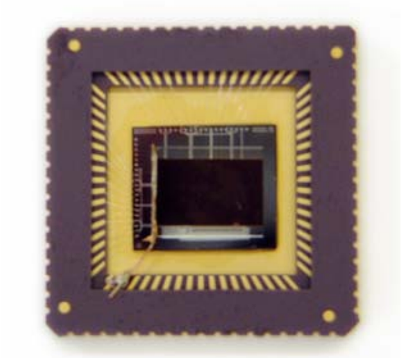


Fig. 5 Sample of CMOS image sensor overlaid with a photoconversion layer by using the microbump method

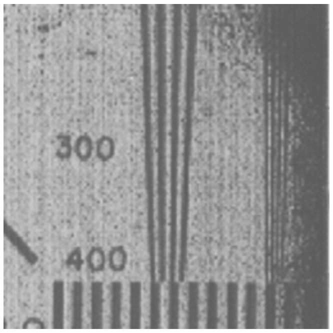


Fig. 6 Reproduced image
Indium-microbump method
(conventional)

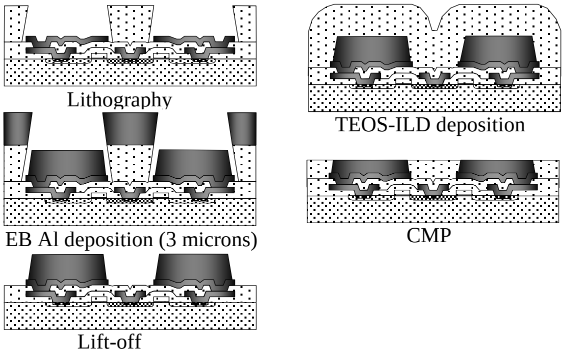
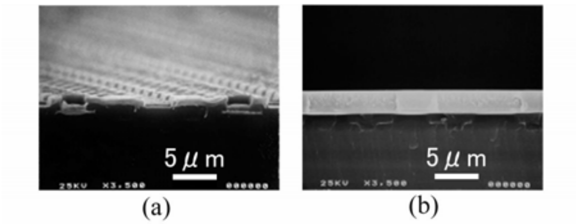


Fig. 7 Aluminium pillar process



(a)
(b)

Fig. 8 SEM images of cross-sectional MOS readout circuit (a) before CMP, (b) after CMP

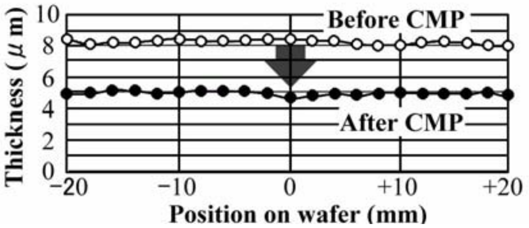


Fig. 9 Global uniformity of surface flatness

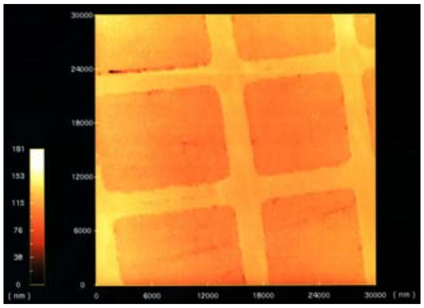


Fig. 10 Local planarity (AFM)

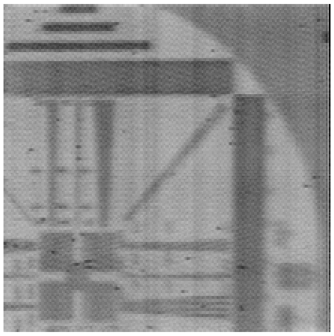


Fig.11 Reproduced image of direct-evaporating method (CMP applied)