The Design of a CMOS APS for Particle Tracking

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Abstract

This article presents the design aspects of the Monolithic Active Pixel Sensors (MAPS) fabricated in a standard CMOS process for charged particles tracking. Integrating the detector and the readout electronics on the common, standard for a CMOS process, low-resistivity silicon substrate, results in a thin (reduced scattering effects) device with high spatial resolution. The fabrication cost, using a standard process, is considerably reduced. As for a classical APS imager, the individual pixel is comprised of only three MOS transistors and the readout electronics is placed on the chip sides. The active detection volume is a thin undepleted epitaxial layer underneath the readout electronics. In this way, the whole detector area is sensitive to particles, providing a 100% fill factor. This papers deals with issues on physics device simulations, noise optimisation, radiation hardeness and tracking performance. Also, a new method of calibrating the charge-to-voltage conversion gain is presented.

I. Introduction

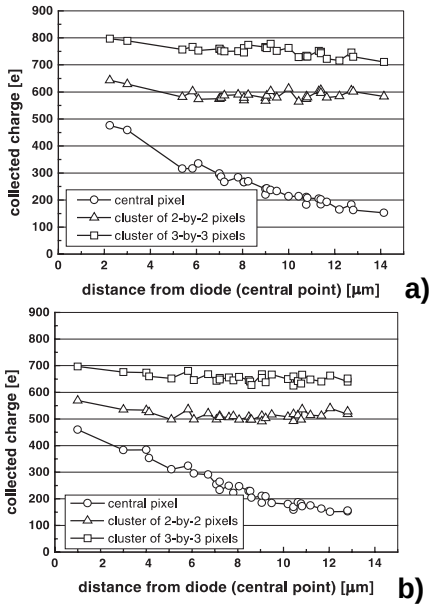
The charge, generated by the impinging particle, is tightly confined to the track, and for minimum ionising particles (MIP) it comes to about 80 e/h pairs/μm. The signal in the APS detector exposed to the particle flux is sensed as a weak and short charge pulse, close to the impact point, coming up on the collection diodes. The detector operates basically 'in the dark', receiving only sporadic hits, but its whole area must be sensitive, providing 100% of the detection efficiency. For the considered detector, based on the charge collection from the epitaxial layer [1,2,3], the total amount of the available charge depends on the thickness of this layer. The charge liberated in the highly doped substrate is mostly lost due to recombination. Only little part of this charge can be gained. On the other hand, the common tendency with scaling down the technology feature size is to reduce the thickness of the epitaxial layer. This translates successively into less total charge which is collected, and increases a percentage of the 'substrate charge' in it. Since there is no strong electric field, the charge, liberated after the impact, diffuses at thermal velocities towards the collecting diodes. Depending on the capacitance of the charge-collecting element, this usually yields less than 20 mV of the total signal per particle. The dynamic range of the detector and its conversion linearity are of less importance for tracking applications. The detector occupancy is usually very low and it is mainly due to the background events, like synchrotron radiation, beam-gas interactions, beam hallo, etc. (e.g. for the TESLA collider, less than 0.1 hits/mm^2/bunch crossing is expected). The segmentation of the detector is determined by the single-track precision and the track separation capability (e.g. within the core of high-energy jets) requested by the experiment. The demanded spatial resolution for nowadays applications is within the range of 10 - 15 μm and it is about 3 μm for the future TESLA linear collider. In some applications, it is acceptable to accumulate the signals over a number of bunch crossings. This can be done for a low signal occupancy leaving events separation to the later data processing. This mode of operation is straightforward for the APS devices that have natural signal integrating capability. An important issue in the design is its radiation hardness, which can be demanded as moderate (TESLA - 20 kRad/year and 10^9 /cm^2/year 1 MeV equivalent neutrons), strong (BELLE - 500 kRad/year) and harsh (LHC - 10^{14} /cm^2/year 1 MeV equivalent neutrons). For the successful design, the detailed noise optimisation, taking into account the actual working conditions i.e. readout frequencies and single pixel sampling, is mandatory. Practically, equivalent charge noise levels well below 10 e$^-$ are now affordable.

II. Charge Collection Physics Simulation

The charge collection efficiency of the MAPS detector has been verified using the ISE-TCAD package [3,4]. The device, described in three dimensions by a mesh generated using the analytical description of doping profiles and the boundary definition corresponding to the real

device, was examined by the mixed mode device and circuit simulator DESSIS-ISE. The charge collection was traced as a relaxation process of achieving the equilibrium state after introducing an excess charge emulating passage of the ionising particle. Different detector parameters, including the thickness of the epitaxial layer, the size of a pixel and collecting diodes and number of diodes per pixel, were investigated.

The sample results in figure 1 show the charge collection for 20 μm pixel pitch and 3x3 μm^2 diode size and accordingly for 15 and 5 μm of the epitaxial layer. All plots in figure 1 are done for the case of a single collecting diode per pixel. The substrate contribution was verified to be limited only to its first 10 – 15 μm, the charge liberated deeper is lost due to recombination. The substrate contribution to the total signal was estimated to be of less importance for a thick epitaxial layer, but when this zone becomes thinner, which is the case for submicron processes, it can even make 50% of the total collected charge. The charge cloud spreads among the adjacent pixels and this effect becomes wider for the thicker epitaxial layer. The collection time was estimated to be within the range of 70 - 250 ns for the 3-by-3-pixel cluster and for the epitaxial layer ranging from 5 to 25 μm. The simulated parameters were verified exposing two prototype chips MIMOSA I and II to the high-energy pion beam at CERN [3] (figure 2).



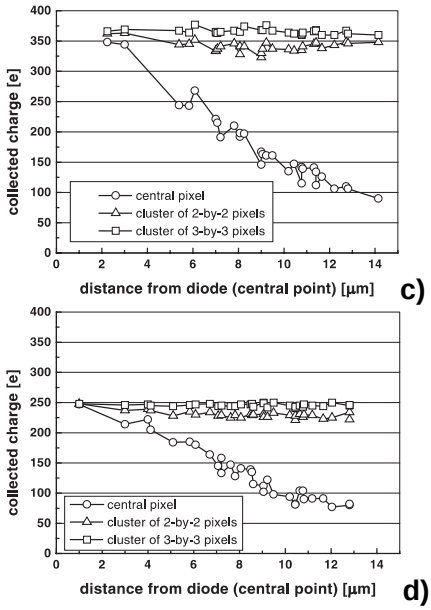


Fig. 1: The simulated charge collection efficiency; substrate of 15 μm thickness -a), -c) and without substrate -b), -d) as a function of the distance between the impact position and the pixel centre for 15 μm -a), -b) and 5 μm -c), -d) thick epitaxial layer

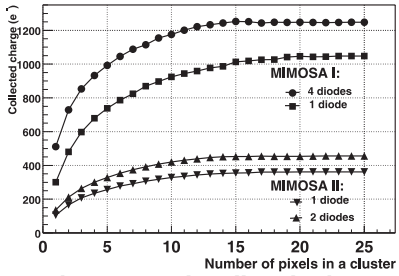


Fig. 2: The measured collected charge (most probable value for MIPs) as a function of the cluster size for two chips having 14 μm and less then 5 μm of the epitaxial layer, number of diodes in a single pixel varies from 1 to 4, the pixel pitch of 20 μm

III. Radiation Hardness

In order to satisfy radiation hardness requirements, the special layout technique with enclosed gates for NMOS transistors was applied. In this design, the transistor effect present in standard rectangular transistors due to the positive charge trapped at the gate ends (bird's beaks), is eliminated. Each NMOS transistor having its exterior terminal adjacent to another transistor at different potential was enclosed by the p^+ guard-ring to prevent surface leakage currents after the type inversion. The noise optimisation and enclosed transistor layout translate to the single pixel size of 8x8 μm^2 in a 0.25 μm process. Although, the aforementioned technique improves radiation

hardness of the electronics, the sensor itself still suffers from radiation effects [5]. For further improvement on the radiation hardness, a special pixel configuration with an extended n^+ region and adjacent p+ implantation areas is proposed. The obtained structure is meant to prevent leakage currents due to the positive charge trapped after high doses of ionising irradiations in the oxide areas of the shallow trench isolations (STI).

V. Noise Performance

The Correlated Double Sampling (CDS) signal processing is a very useful tool allowing signal extraction no matter how strong are the leakage currents or the DC-level pixel output fluctuations after resetting. The latter is seen by CDS as a DC component and leakage currents are suppressed as pedestals. The shot noise caused by the leakage current is usually non dominating. CDS modifies the noise spectral density, and aliasing effects may occur when the sampling frequency is below the noise bandwidth. Basically, CDS improves the signal-to-noise ratio by suppressing the kTC noise, which dominates other noise components, however the thermal noise contribution increases. This is why in a designer's interest is to limit the bandwidth of the pixel source follower e.g. by loading the output line with some extra capacitance. The traded-off in the readout speed can be made up for in an alternate column readout [3]. In contrast to column-level CDS, which is commonly used in photo-applications, the only method not leading to signal loss is to process the whole frames. This approach works at the price of either more extended hardware (on pixel, on chip or external frame-capacity memory) or a very fast transfer link with an external CDS processing. The external memory cannot be accepted, as it increases the material budget close to the interaction point. The idea of the fast ADCs and hardware processors in the VME crate is proposed as a quick start solution. The detailed noise analysis, taking into account the observed in deep submicron processes increase of noise coefficients for transistors with minimum gate lengths and for the strong inversion region of operation, was performed. The obtained results are shown in figure 3. The ratio of the charge-to-voltage conversion gain to the total output-referred noise after CDS processing for different bias currents of the pixel source follower is plotted versus the gate length of the source follower transistor. In Figure 3, the noise contribution only of the latter is depicted. The optimum gate length is shifted when the column current source and the output amplifier are included. For the optimum bias conditions the noise level below 6 e^- was achieved for 20MHz readout. This factor goes with the conversion gain of ~13.1 μV/e^- for 0.47 μm long gate of the follower transistor in 0.25 μm process.

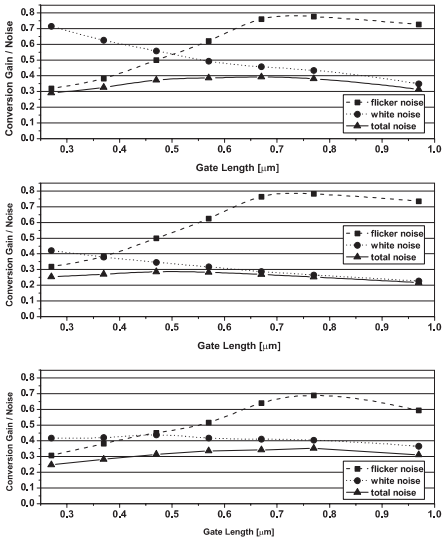


Fig. 3: The ratio of the conversion gain to the total output-referred noise after the CDS processing for the optimum 20μA -a) and then for 5 μA -b) and 50 μA of bias current calculated for a 0.25 μm process design, the contribution of the source follower transistor is only depicted and 10MHz analogue readout.

The position calculation algorithms take into account charge spreading onto adjacent pixels. The precision computation depends on the cluster signal-to-noise ratio. In order to decrease the cluster noise (square root of the number of involved pixels times the single pixel noise) a non-squared i.e. staggered array layouts were used. In this case tighter covering of the active volume by collecting diodes would preserve good charge collection efficiency.

IV. Calibration of the Conversion Gain

The commonly used method of the charge-to voltage conversion gain calibration for the APS device is based on the Poisson statistics of the integrated shot noise. The conversion gain is estimated from the transfer curve of the squared pixel noise (after CDS) upon the measured average signal over certain number of the acquired images. The conversion gain can also be estimated analysing emission spectra of a low energy X-ray source. In this case, the iron ^{55}Fe source emitting 5.9 keV photons was used. For such photons, having the attenuation coefficient

about 140 cm^2/g, the detection efficiency is very high even for thin detection volumes. Due to the photoelectric effect, neglecting other energy losses but ionisation, a constant number of charge carriers, i.e. 1640 e/h pairs per one 5.9 keV photon, is generated in silicon. Because of the charge transport mechanism by thermal diffusion, the average charge collection for each pixel is only partial. The assumption of fully efficient collection is justified only for a small sub-sample of photons converted close to the depleted volume of the diode p-n junction. The obtained energetic spectra for the seed pixel, exhibiting the highest signal-to-noise ratio in the cluster, are presented in figure 3. The second, small peak was used to measure the conversion gain. Thorough analysis shows no charge collected onto the adjacent pixels confirming previous assumptions on the full collection efficiency. The obtained conversion gain values for the MIMOSA I prototype were 14.6 $\mu V/e^-$ and 6.0 $\mu V/e^-$ after pixel source follower, respectively for the design with one and four collecting diodes. These measurements preceded by hand-made calculations were also verified using the statistical method in parallel.

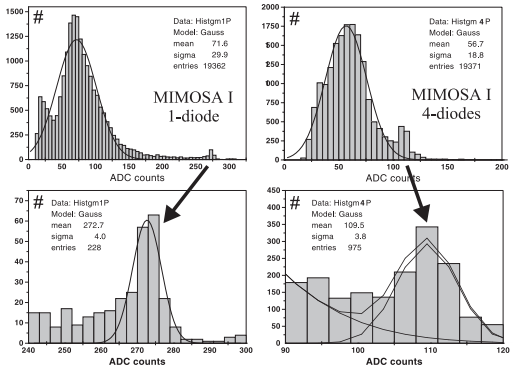


Fig. 3: Measured 5.9 keV photons spectrum on the seed pixel in the clusters in the case of 1 and 4 diodes per pixel, the bottom histograms show the second peak which is taken as reflecting 100% collection efficiency

V. Tracking Performance and Conclusions

Two already fabricated prototype chips with active arrays of 64x64 pixels laid down with the pitch of 20 μm were tested. The measured tracking performance for MIPs [3] is characterised by the detection efficiency close to 100%, the cluster signal-to-noise ratio of more than 30 and the spatial resolution in the range 1.5 – 2.5 μm (figure 4). The next step is to design a big macrostructure (~2x8 cm^2), which could be used in the real vertex detector. Figure 5 shows a schematic study of such a detector slab. This design will need to deal with many technological and engineering (like on-wafer stitching, reducing the chip surface occupied by "non active electronics") as well as data processing problems (on-chip data reduction and compression). The first step to be realised is to introduce CDS processing on-chip. Some ideas with voltage and current mode analogue memories on the pixel level are under study. This requires signal subtraction amplifiers at the columns ends and the parallel or multiplexed pixel outputs, but the non-active chip space will be limited to a few percent close to one edge only (figure 5).

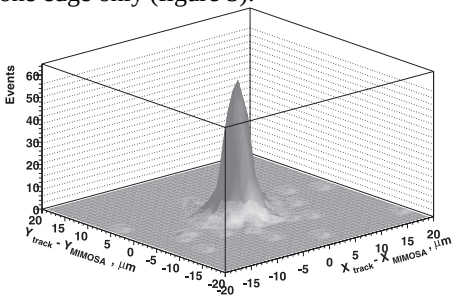


Fig. 4: 2D distribution of position of all reconstructed clusters with the respect to the reference tracks for the prototype chip having 14 μm of the epitaxial layer.

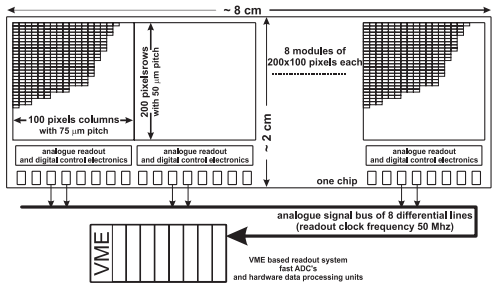


Fig. 5: Proposal of a single-chip detector

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