

# Column Parallel A/D Conversion on CMOS Image Sensor

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## ABSTRACT

We describe a CMOS image sensor with column parallel Analog to Digital Conversion circuits. In this sensor, small 1bit comparator for each column is used for 8 bit A/D conversion. The processing of our proposal is divided into 4 steps during the integration of PD value and 2 bit of pixel value is determined at each step. Therefore 8 bit value is determined when the integration is finished.

We have designed a first prototype by using  $0.6 \mu\text{m}$  CMOS process and a second prototype by using  $0.8 \mu\text{m}$  CMOS process. The prototypes output analog value and 8 bit digital value of pixel data. We describe the method of proposed ADC and the design of the prototypes. We show results of the experiment obtained by the first prototype.

## I. Introduction

We have been investigating the smart image sensor which is integration of sensing and processing on a LSI chip[1]–[3]. The integration of sensing and processing makes use of parallel nature of image signal on the focal plane so that the processing gets remarkably faster compared to ordinary image processing systems which are based on a traditional sense-read-and-process paradigm.

In this paper, we describe a new on-sensor analog to digital conversion (ADC) technique. 8bit ADC can be done by using column parallel 1bit comparator which detects each bit during integration of pixel value. Because each column shares 1bit comparator, the area of column parallel ADC circuit is much smaller compared to the conventional on-sensor ADC image sensor.

We have designed two prototypes by using column parallel architecture. The first prototype has  $32 \times 16$  pixels and the second prototype has  $64 \times 32$  pixels. We describe the processing scheme of our ADC, simulation results, and the design of the prototypes.

## II. On-sensor A/D conversion

Figure 1 shows three architectures of on-sensor ADC, which are single, column parallel and pixel parallel ADC circuits. In the case of single ADC circuit, the sensor has PD array and column parallel readout circuits and one ADC circuit. Because PD cell keeps high fill factor and all pixels shares one ADC circuit, the quality of output image is very good. But, the ADC is required for high speed processing and it can not operate at higher frame rate.

The column parallel architecture has the PD array and column parallel ADC circuits and readout circuits. PD cell also keeps high fill factor. The pixels on each column shares one A/D conversion circuit so that the processing is fast.

The other architecture is pixel parallel ADC circuits. Each pixel has ADC circuit so that it is able to make use of two dimensional nature of image signal. Therefore the processing is very fast. But this architecture has disadvantage of the low fill factor and high power dissipation.

In this paper, we adopt the column parallel architecture for our image sensor. Figure 2 shows the digital smart image sensor we have been investigating. The sensor is divided into 4 elements. They are PD array, digital memory array, ADC circuits and digital processing circuits. Each column shares small 1 bit ADC circuit which is capable for 8 bit A/D conversion. 1 bit comparator determines 2 bit of pixel value at each steps, repeatedly. In this sensor, transducing, A/D conversion and processing can be done in parallel.

The processing of our proposal is divided into 4 steps (s1,s2,s3,s4) during the integration of PD value, as shown in Figure 3. 2 bit of pixel value is determined at each step. Therefore 8 bit value is determined when the integration is finished. Because we use 1 bit comparator for 8bit A/D conversion repeatedly, the processing circuit of A/D conversion is very small.

In our proposal, the interval of each step is not

equal. The processing of s1, s2, s3, s4 is done when the integration time is 1/8, 1/4, 1/2, 1 frame, respectively. By this scheme, the number of the reference values are reduced from 14 to 8 so that the peripheral circuit to make the threshold voltage is also small. Table 1 shows the reference values for each sub-frame.

Figure 4 shows an example of the proposed method when the final pixel value is 200. Because the object is not moving, pixel values for s1, s2, s3 and s4 are 25, 50, 100 and 200, respectively. Table 2 shows the threshold of each step and the result of A/D conversion.

### III. Computer simulation

Figure 5 shows the simulation results of our A/D conversion when the speed of the object is from 8 pixels / frame to 128 pixels / frame. We make the moving sequences by using two HDTV still images. In this figure, the conventional method means A/D conversion after integration. It appeared that the results of the proposed method is much clear compared to the conventional approach. In our proposal, higher bit (ex. MSB) is determined when the integration time is shorter. Therefore the motion blur is reduced as shown in Fig.5.

### IV. Design of on-sensor A/D conversion

We have designed two prototype chips based on column parallel architecture. Figure 6 shows the block diagram of the on-sensor A/D conversion. The prototypes are divided into three part which are transducer array, 8bit digital memory array and A/D conversion circuits. The pixels on each column shares one A/D conversion circuit. Using two vertical shift registers, the pixels and the memories are scanned line by line.

### V. First prototype chip and experiment

Table 3 shows the outline of two prototype chips. The first prototype chip is fabricated by 2-poly 3-metal 0.6  $\mu\text{m}$  CMOS process. The sensor has 32 x 16 pixels and fill factor is 41.2%.

Figure 7 shows the analog output images obtained by the prototype when “sensor” is moving from right to left.

### VI. Second prototype chip

We have designed the second prototype chip because the first prototype does not output digital pixel value well. As shown in Table 3, the second prototype is

designed by 2-poly 2-metal 0.8  $\mu\text{m}$  CMOS process rule. The sensor has 64 x 32 pixels and fill factor is 39.1%.

Figure 8 shows the circuits of the second prototype. Each pixel has only a transducer and a separate corresponding 8bit digital memory and a processing circuit shared by the pixels on the column. The processing circuit has sample & hold circuit, comparator, temporal 2 bit memory, D/A converter and switch circuit. Power circuit supplies the reference voltage for D/A converter in the processing circuit. The second prototype is in fabrication.

### VII. Conclusion

In this paper, we propose a new method of on-sensor A/D conversion for digital smart image sensor. We have designed and implemented a first prototype chip which has 32  $\times$  16 pixels. We have also designed a second prototype chip which has 64  $\times$  32 pixels.

### VIII. References

- [1] K.Aizawa, T.Hamamoto, Y.Ohtsuka, M.Hatori and M.Abe, “Implementations of On Sensor Image Compression and Comparisons between Pixel and Column Parallel Architectures”, *IEEE ICIP97* Vol.2, pp.258–261 (1997)
- [2] T.Hamamoto, Y.Ohtsuka, K.Aizawa, “Very fast tracking and depth estimation by using focal plane compression sensors”, *IEEE ISCAS'99*, vol.IV, pp.127–130 (1999-6)
- [3] T.Hamamoto, K.Aizawa, “A computational image sensor with pixel-based integration time control”, *IEEE ICIP'00*, Vol.I, pp.729-732 (2000.9)

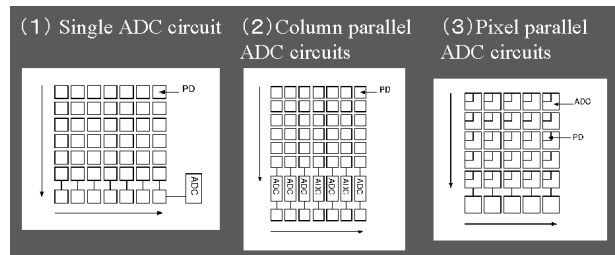
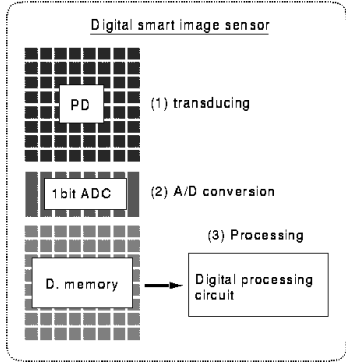
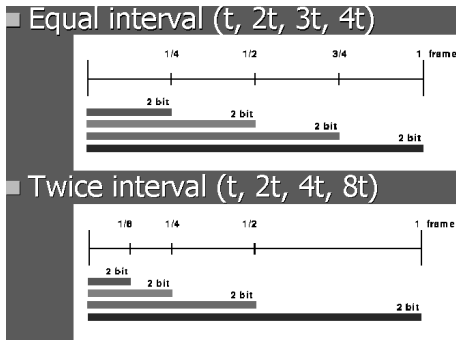


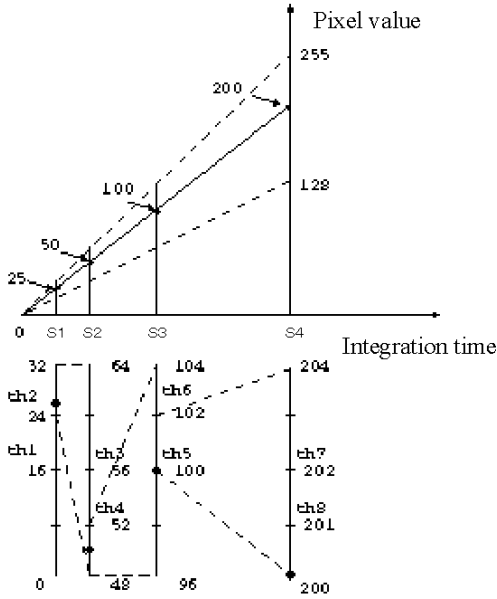
Fig. 1. Architecture of on-sensor ADC



**Fig. 2.** Proposed on-sensor ADC for smart digital sensor



**Fig. 3.** Comparison between equal and twice intervals for 4 steps ADC



**Fig. 4.** Example of our ADC method when the pixel value is 200

**Table 1.** Reference potential for each sub-frame

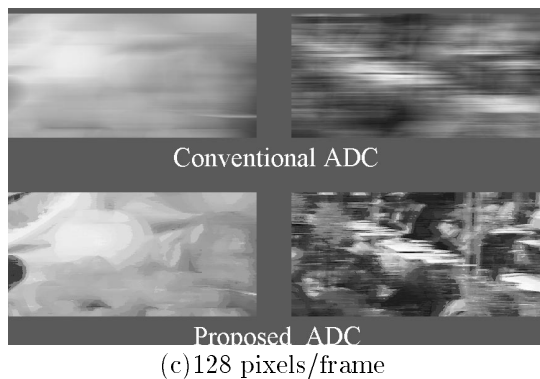
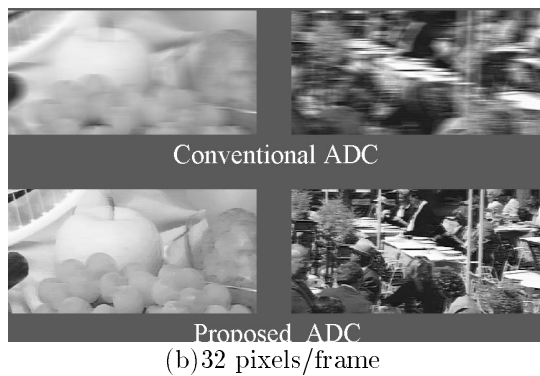
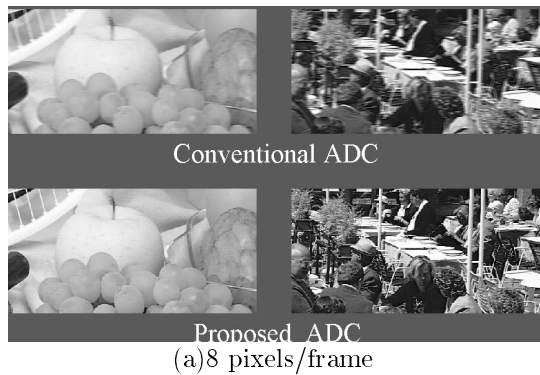
	MSB							LSB
	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1
s1(1/8)	16	8						
s2(1/4)	32	16	8	4				
s3(1/2)	64	32	16	8	4	2		
s4( 1 )	128	64	32	16	8	4	2	1

**Table 2.** Threshold of each bit and the result of ADC

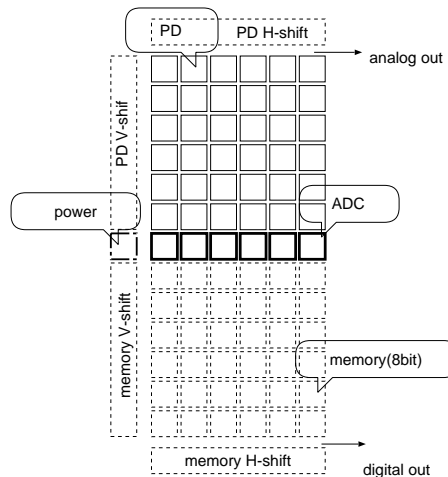
	MSB							LSB
	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1
result	1	1	0	0	1	0	0	0
s1 th1	16							=16
(1/8) th2	16	+8						=24
s2 th3	32	+16	+8					=56
(1/4) th4	32	+16	0	+4				=52
s3 th5	64	+32	0	0	+4			=100
(1/2) th6	64	+32	0	0	+4	+2		=102
s4 th7	128	+64	0	0	+8	0	+2	=202
( 1 ) th8	128	+64	0	0	+8	0	0	+1 =201

**Table 3.** Outline of the prototypes

	first	second
number of pixels	32 × 16	64 × 32
process(μm)	0.6	0.8
chip size(mm <sup>2</sup> )	4.5 × 4.5	5.2 × 9.1
transducer(μm <sup>2</sup> /pixel)	20 × 20	60 × 60
memory(μm <sup>2</sup> /pixel)	63 × 73	60 × 150
processing(μm <sup>2</sup> /column)	63 × 615	60 × 618
transducer(Tr./pixel)	3	3
memory(Tr./pixel)	72	80
processing(Tr./column)	266	232
fill factor(%)	41.2	39.1
power (V)	5	5



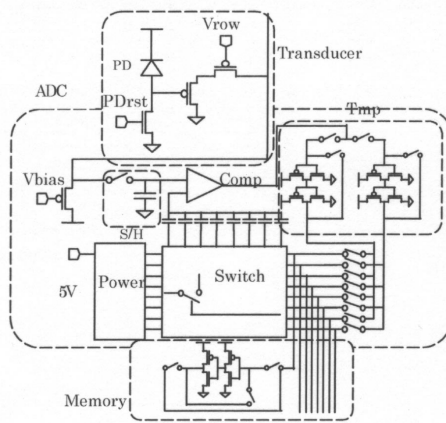
**Fig. 5.** Simulation result of A/D conversion when moving speed is 8, 32, and 128 pixels/frame, respectively; conventional method: pixel intensity is determined after integration, proposed method: pixel intensity is determined during integration.



**Fig. 6.** Block diagram of the prototype chips



**Fig. 7.** Analog output images obtained by the first prototype (characters of "sensor" are moving.)



**Fig. 8.** Circuit for a pixel of the second prototype