

Intra-Pixel Reset Noise Cancellation

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Abstract

Suppression of reset noise in CMOS image sensors can reduce the noise floor to a level that is competitive with CCD sensors. The most commonly used technique for reset noise reduction in CMOS sensors is the pixel that behaves like a CCD output stage [1], [2]. However these types of pixels have a number of problems, including lower blue response because of the CCD structure, higher readout power and delay due to the double read cycle, non standard processing, and column noise if the cancellation circuits are at the column ends. In this paper we describe a reset noise cancellation pixel that solves all these problems, using a reset noise cancellation circuit within the pixel.

Principle of Operation

Figure 1 shows the pixel schematic, and figure 2 shows the timing diagram. At the beginning of the exposure cycle, N2 and N6 are both on, holding nodes 1 and 3 at quiet reference potentials. Node 2 is driven to a level about one V_{TN} below the level of node 1, by the N3 / N4 source follower buffer. Next N2 turns off, leaving a noise voltage of $\sqrt{kT/C1}$ on node 1. This noise voltage will also appear on node 2, attenuated by the gain of the source follower pair N3 / N4. However node 3 still remains clamped to V_{ref2} by N6 during this time.

When N6 turns off, a noise voltage of $\sqrt{kT/C2}$ is left on node 3. This noise voltage can be made arbitrarily small by choice of the C2 value, without effecting the sensitivity of the pixel. After N6 turns off, integration of light can begin by opening the shutter (global or rolling shutter can be used with this type of pixel). Current from the photodiode passes through the barrier gate N1 onto the charge to voltage conversion capacitor C1. The purpose of N1 is to minimize the capacitance of the charge to voltage conversion node C1.

As node 1 drops in response to the photocurrent signal, node 2 follows. Since C2 is large compared to other capacitances on node 3, node 3 tracks node 2. At the end of the integration interval, node 3 has a voltage equal to the collected photo charge divided by C1, times the gain of the source follower pair N3 / N4. But the reset noise is $\sqrt{kT/C2}$, which can be much smaller than the reset noise of C1, which is a very small capacitor. So high sensitivity is achieved along with low noise.

Transistors N7 and N8 form the output source follower and row select function commonly seen in CMOS pixels.

Circuit Parameters

A C2 value of 100 fF can reduce the pixel output noise down to the level of other noise sources in the pixel, such as source follower 1/f noise (about 100 μ V). In a 0.18 μ m process, which has the thinnest gate dielectric compatible with image sensors, 100 fF occupies about 10 μ m² of pixel area, about 10% of the pixel area for a high quality still camera sensor. Embedded DRAM capacitors (about 40 fF / 0.25 μ m²) could also be used for this purpose if available.

C1 is made as small as possible to maximize the sensitivity of the pixel. The value of C1 is measured by comparing the photo current seen at V_{ref1} to change in pixel output level, after accounting for gain from node 1 to the output. C1 measured this way was 1.4 fF. Pixel gain is measured by comparing the change of a voltage forced at V_{ref1} to change in pixel output voltage, and is about 0.50. Sensitivity can be calculated from pixel gain and sense node capacitance, and is about 57 μ V / electron.

Because Capacitor C2 is made using an nmos transistor, care must be taken to ensure N5 is biased to remain in inversion mode, that is the voltage on node 3 must exceed the voltage on node 2 by one VTN at all times. Fortunately there is also a drop of one VTN from node 1 to node 2, so the levels of V_{ref_1} and V_{ref_2} can be about the same. In fact, to minimize array wiring, V_{ref_1} , V_{ref_2} and V_+ can be the same node. Maximum voltage of this positive supply is limited by acceptable leakage current on node C1, which depends on the application.

V_{bias} is chosen to provide enough current in the source follower buffer N3 / N4 to meet the settling time requirements of the sensor. For a C2 value of 80 fF, and a bias current of 1 nA, slew rate is 1 Volt / 100 μ sec, adequate for many imager applications. 1 nA of bias current will allow for megapixel arrays with acceptable power levels.

V_{bias} also has an effect on the fixed pattern noise of the sensor, which is higher with this type of pixel because there are more sources of variability. A global dark frame taken with a mechanical shutter is one simple way to accomplish first order cancellation of fixed pattern noise. It should be noted that because the temporal noise cancellation circuit is inside the pixel instead of at the end of the columns, the cancellation circuit cannot add column or row noise.

Experimental Results

Figure 3 shows the layout for the pixel which was evaluated. It was built with a 0.25 μ m, five layer metal CMOS process. Figure 4 shows the blue response for an n-well / p-substrate diode on this process, which is relatively flat from 400 nm to 700 nm.

Noise measurements were made by loading the pixel output with a capacitance similar to the amount of column capacitance seen in an array. The pixel output was then sampled with a digitizing oscilloscope, and approximately 1000 sam-

ples are captured and stored. Noise reported here is the standard deviation of these sampled values.

Table 1 shows the results. Data in column I is the noise baseline, most of which is system noise. This is obtained by holding N2 and N6 in hard reset mode. Column II is the noise of the dark level after the switches have been turned off. Column III is the incremental added reset noise, calculated from the baseline noise and the dark level noise. The three pixel types in table 1 correspond to three different pixel layouts, with different C2 implementations. The reduction in reset noise can be seen in Column III, as a function of the value C2.

Figure 5 shows how photon shot noise compares to reset noise near the dark level, for pixel type A (no noise cancellation) in table 1. Note that photon shot noise becomes comparable to reset noise at fairly low signal levels, especially if noise cancellation is to be used.

Conclusions

In this paper we have explored the issues associated with an intra-pixel reset noise cancellation circuit. This technique can be implemented in a reasonable amount of silicon area, with standard CMOS process, and achieve a significant reduction in reset noise. Also this pixel can have good blue response, and low column fixed pattern noise. The disadvantage is that DC power is consumed, and random fixed pattern noise will increase.

[1] Guidash et Al., "A 0.6 μ m CMOS Pinned Photodiode Color Imager Technology", IEDM 1997 page 8.8.1

[2] Mendis et Al., "Progress in CMOS Active Pixel Image Sensors", SPIE volume 2172 page 19

[3] Fowler et Al., "Low Noise Readout using Active Rest for CMOS APS", SPIE Volume 3965 page 126

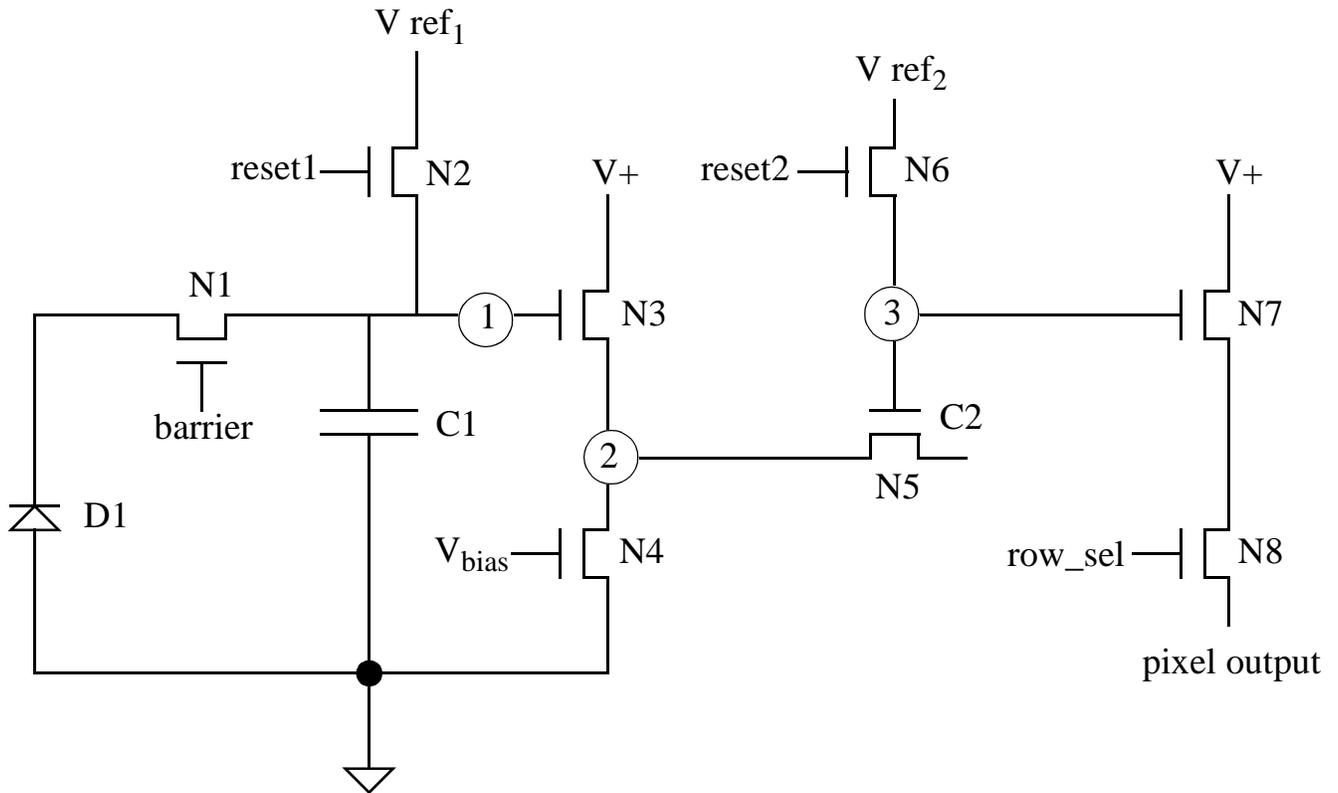


Figure 1. reset noise cancellation pixel

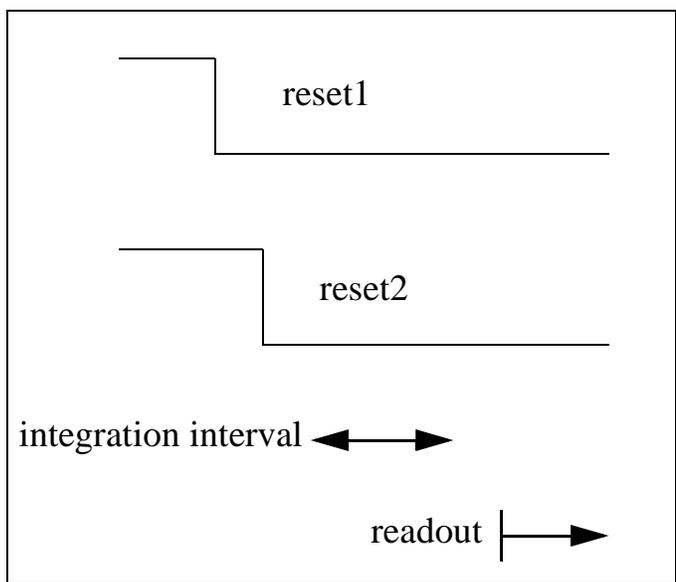


Figure 2. pixel timing

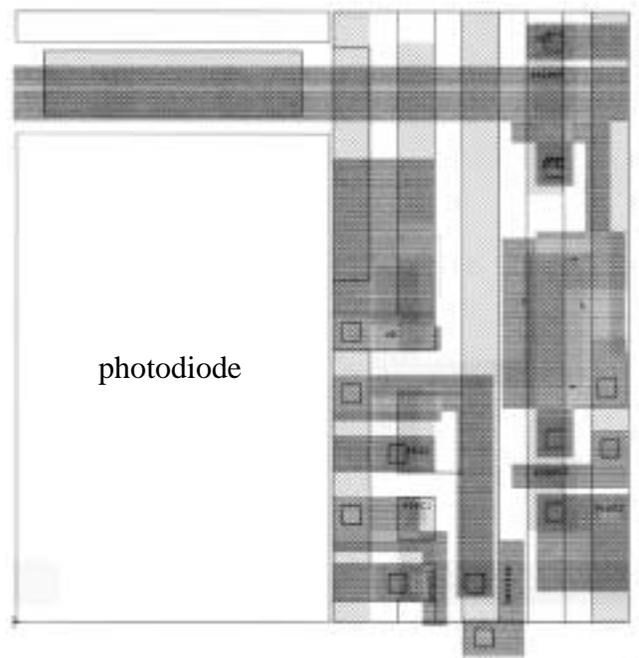


Figure 3. pixel layout

Table 1: reset noise cancellation pixel results

pixel type	pixel description	I $v_1 =$ noise during hard reset mV	II $v_2 =$ noise of dark level mV	III $v_3 =$ reset kTC noise mV (1)
A	no noise cancellation C2 = short	0.42 (2)	1.11	1.02
B	noise cancellation pixel C2 = 10 fF	0.39	0.67	0.52
C	noise cancellation pixel C2 = 80 fF	0.31	0.36	0.18

(1) $v_2^2 = v_1^2 + v_3^2$

(2) measured noise at the pixel output; noise at C1 is divided by the total amplifier gain = 0.5X

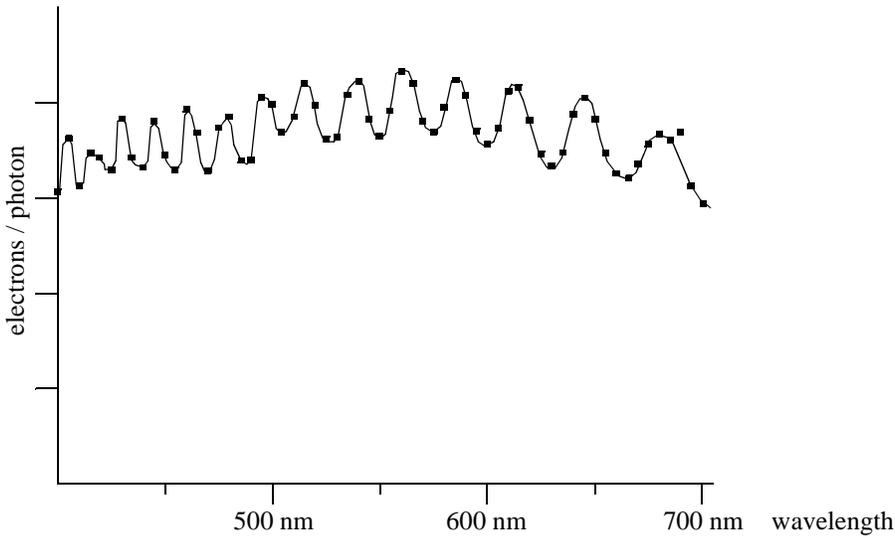


figure 4
blue response of n-well photodiode

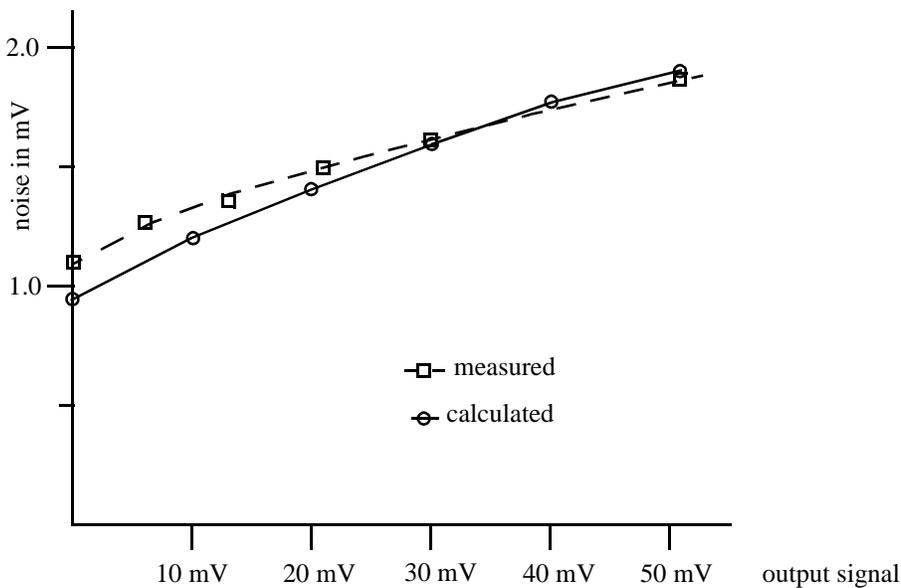


figure 5
comparison of photon shot noise to reset noise