A 6.6Mpixel pixel CMOS image sensor for electrostatic PCB inspection

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Abstract

This paper discusses a CMOS image sensor used as an electrostatic field detector to be used in a fine pitch PCB and flex circuit inspection system. The design consists out of a 3170x2120 three transistor active pixel array and on chip Fixed Pattern Noise correction circuitry. The sensor measures about 37x25 mm^2 and is designed in a 0.5 μm technology using stitching techniques.

I Introduction

In light sensing applications, a lens projects the image on the sensor’s surface. In this case however, were an electric field is the ‘light source’, a lens does not make a lot of sense. During the image acquisition, the PCB to be tested is pressed to the sensor’s surface and during readout, an electric pulse is applied to the PCB tracks. In this way the electrostatic field induces an image on the pixel array through capacitive cross talk from the PCB to the pixels. Figure 2 clarifies the principle. Compared to visual inspection this approach has the advantage that if a lane on the PCB is interrupted, it will result in large parts missing in the images rather than small and hard to detect dark regions. Next to this, the large size of the pixel array allows multiple PCBs to be tested simultaneously, or larger PCBs to be tested compared to standard size sensors. The next sections discuss the pixel and sensor architecture, stitching issues and measurement results.

II How to detect and electrostatic field?

To detect the electrostatic field, an electrical pulse is applied to the test pattern. This pattern, forming one plate of the coupling capacitor, is pushed against the sensor’s surface and by doing so, the field is ac-coupled into the pixels. The pixel architecture is based on the classical three-transistor pixel shown in Figure 1, in which the photodiode, normally used to detect light is replaced with a large top metal plate, the second plate of the coupling capacitor. The quality of the capacitive coupling is determined by the ratio between the coupling capacitance (C_c) and the parasitic capacitance (C_{pix}). The idea is to minimise the C_{pix} and to maximise C_c. The 11.4 x 11.4 μm^2 pixels contain the three transistors and a 10x10 μm^2 Metal3 plate. The fill factor of this pixel is no longer determined by the size of the photo diode, but by the size of top metal plate compared to the pixel area. In this pixel the ‘fill factor’ is about 75%. The capacitance of the pixel C_p, the distance to the pattern to be tested and the amplitude of the applied pulse determine the sensitivity of the pixel to the electrical pulse. The measured pixel capacitance C_p is about 6 fF, yielding a sensor output signal of 0.6V for a 50V pulse.

$$V = \frac{C_c}{C_c + C_p} V_{in} = \frac{7\times10^{-17}}{7\times10^{-17} + 6\times10^{-15}} \times 50V = 0.6V$$

$$C_c = ee_0 \frac{S}{d} = 4\times8.85\times10^{-12} \times \frac{10^{-5}\times10^{-5}}{50\times10^{-6}} = 7\times10^{-17} F$$

Although the major part of the pixel is already covered by metal, the layout is done in such a way that the light sensitivity is reduced to an absolute minimum. In this way, parasitic incoming light does not influence the acquired images. To ensure an effective collection of all free charges generated by light an *nwell* photodiode is connected to VDD. As a result, the collected charge is deduced to VDD rather than affecting the electrostatically generated image. The spectral response measurement on this pixel proves the feasibility of the concept: maximum QE is about 0.1%, about 300 – 400 times lower compared to a similar sensor optimised for a normal, light sensing, application (Figure 3).

III Sensor architecture

Figure 4 shows the floorplan of the 6.6Mpixel image sensor: first of all there is the pixel array of approx. 3170x2120 pixels, next two shift registers in the vertical, y, direction in combination with the necessary logic control for proper resetting and electronic shutter, and at the bottom the column amplifiers and the x read out shift register. Four amplifiers in parallel buffer the analog output of the sensor to the outside world.

IV Stitching

One of the most important specifications of this sensor is the physical size: the image plane is close to 24x36 mm^2. As this is larger than the maximum reticle size of about 20x20 mm^2, stitching techniques have to be used for the processing of this chip. The sensor can be divided into a number of elementary blocks, each block containing a part of the design. Figure 5 shows how this is done: block F1 has consists out of a partial pixel array (1600x620 pixels) and a section of the vertical shift registers. The same applies for block F4 (520x620 pixels). Blocks F2, F3, F5 and F6 are each unique parts of the design, which are not repeated but of which only one per sensor is used. These blocks contain some pixels, output amplifiers, the start of the *x* and *y* shift registers, column amplifiers, interconnects to the pads etc. Patterns, lines (e.g. reset, select and bias lines) crossing the cut lines are made a bit wider, not following the minimum design rule, to ensure a proper connection from one stitch block to the next. Due to the physical size of the sensor, relatively long interconnect lines are used, having more parasitic capacitance than in a normally sized design. On chip current mirrors are adapted to these larger than normal loads.

V FPN correction?

Fixed Pattern Noise is on chip removed by a double sampling technique. The principle is based on subtracting the reset level from the signal through AC coupling. The principle is based on an amplifier (per column) that is used during calibration as inverting amplifier, and during readout as source follower (Figure 6). This way, the reset and signal level are subtracted using the same amplifier, without adding additional FPN. During the row calibration sequence, the signal levels of the selected row are applied to the column amplifiers. At this time, control signal *S* is low, hence the source of transistor *M* is connected to a reference source. The gate of this transistor now equals this level plus the threshold voltage of transistor *M*, including its non uniformity. Next, S goes high and the column amplifiers are configured as source followers. The reset levels of the selected pixels are now through the AC coupling fed to these source followers, and at the output, the difference, free of FPN is multiplexed to the four parallel output amplifiers. The DC reference of about 1.2Volt is generated on chip. The FPN correction method is discussed more into detail in [1].

VI Output amplifiers

As the sensor does not have on chip Analog to Digital Converter(s), the output amplifiers are designed in such a way that the offset and gain of the output signal can be adjusted to the input range of the external ADCs. Figure 7 shows the basic two step architecture: the first amplifier sets the gain, the second sets the offset. This second stage is a unity gain stage, controlling the bandwidth. The gain stage has a four bit programmable gain ranging form 1.2 up to 18. Using the two step approach ensures a more or less equal bandwidth for all gain settings (Figure 8). Default pixel rate is 10 Mpixels/sec, giving a maximum frame rate of more than 4 full frames per second.

VII Results

The main electrical results are summarised in Table 1. Figure 9 shows the sensor packaged using chip-on-Board techniques. Pictures showing the image quality are shown in Figure 10 and Figure 11.

Table 1. Overview main specifications

Resolution	3170x2120 pixels
Pixel size	11.4 x 11.4 µ m^2
Spectral sensitivity	400 – 1000 nm
Spectral response*fill factor	max. 0.001 A/W
Peak QE * fill factor	0.1% @ λ=500–700 nm
Fill factor	75% (=metal top plate)
Photodiode capacitance	5.8 fF
Conversion factor	27.6 µV/e^-
Output voltage swing	1.7 V @ minimum gain
Full well charge	80,000 e^-
Temporal noise	22 e^-
Dynamic range	2650:1
Dark current	108 pA/cm^2
Dark current signal	8.4 mV/s
Pixel rate	10 MHz
Frame rate	4 frames/s (4 outputs)
Gain output amplifier	Dig. adjustable from 1.2 – 18 x
Supply Voltage	5 V
Power dissipation	215 mW

VIII References

1. Bart Dierickx, Guy Meynants, Danny Scheffer, “Offset free offset correction for active pixel sensors.” IEEE Workshop on CCD and AIS, Bruges, Belgium, June 5-7 1997

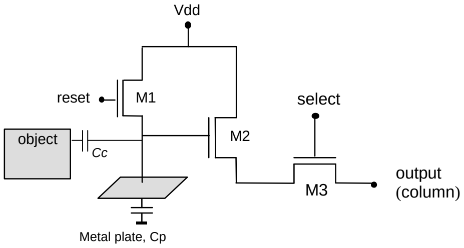

Figure 1. Pixel architecture

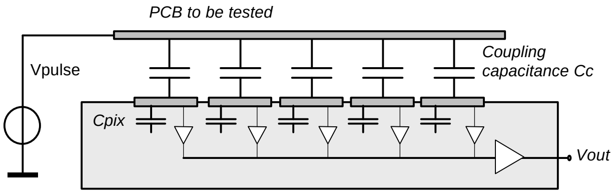

Figure 2. Principle of electrostatic sensing.

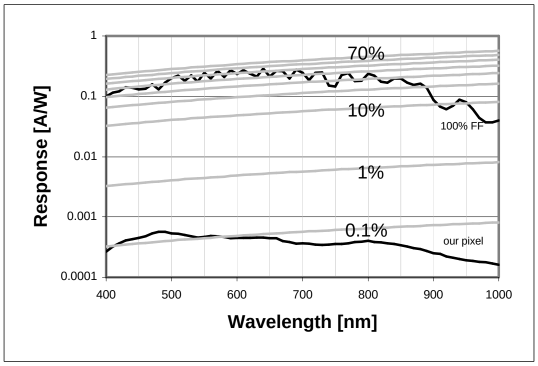

Figure 3. Spectral response curves

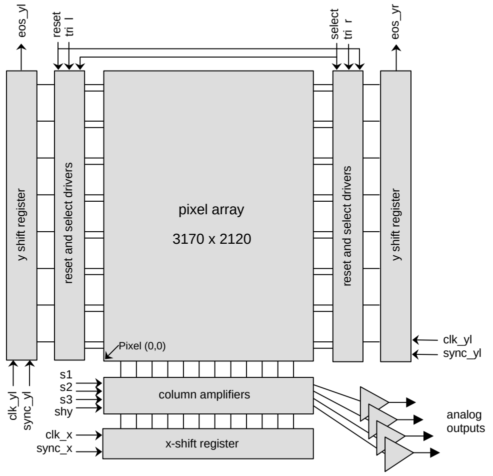

Figure 4. Sensor architecture

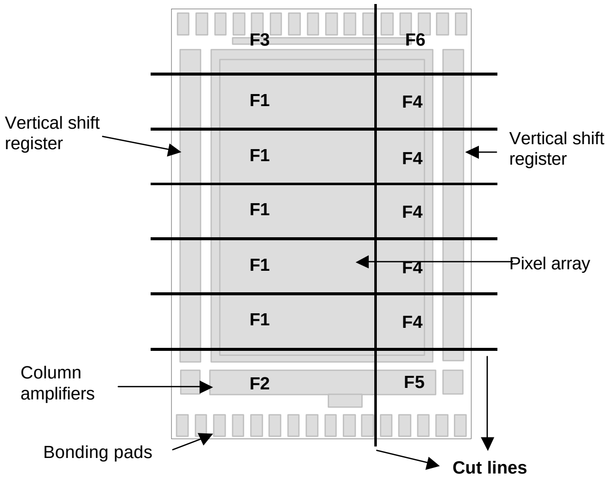

Figure 5. Floor plan and stitching diagram

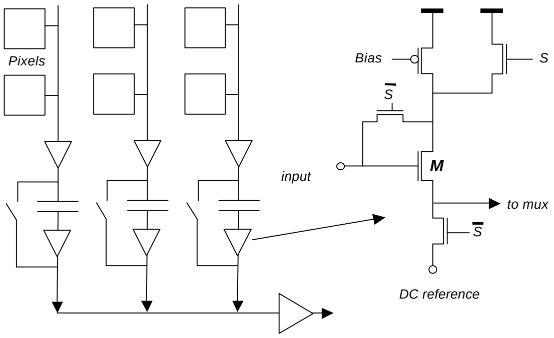

Figure 6. FPN removal circuitry

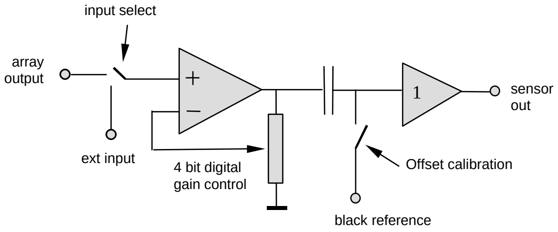

Figure 7. Output amplifier architecture

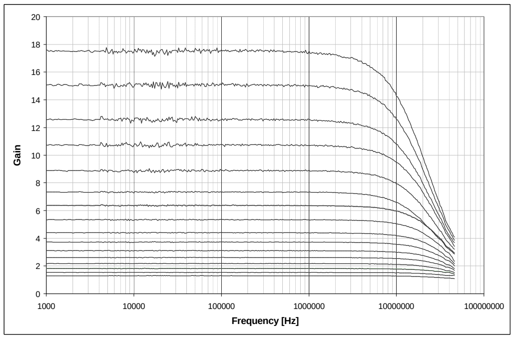

Figure 8. Bode diagrams gain setting 1 – 18x

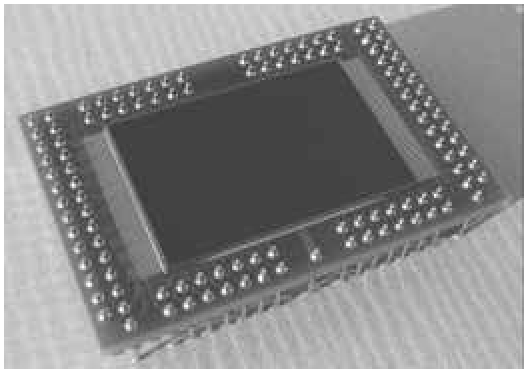

Figure 9. Sensor photograph, evaluation package

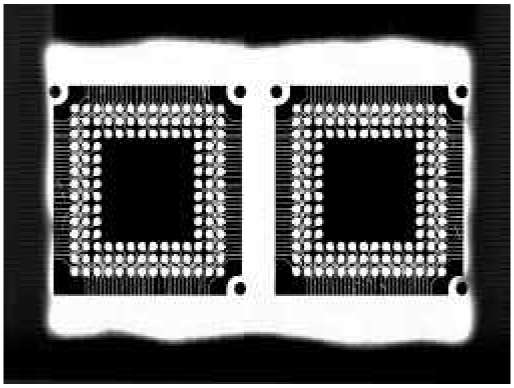

Figure 10. Full sample image

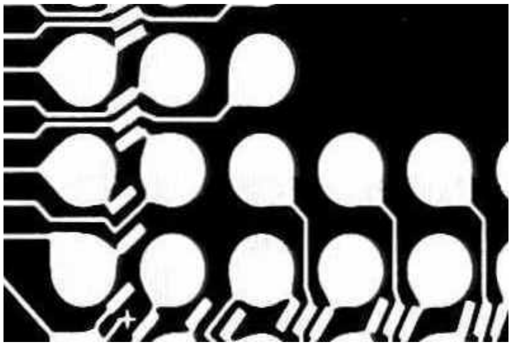

Figure 11. Detail showing clearly all interconnections